Within recent announce by yole the FOWLP CAGR increase by ~55% due to APPLE/TSMC entry. FO-WLP have been seen as emerging platform technology for multi-chip integration, smallest form factor and cost competitive solution. EPTC 2015 have line up a short course on FO-WLP and series of invited papers & speakers to present on the technology. Full details are in the subsequent pages.
**Professional Development Courses**

Professional Development Course 1  
2\textsuperscript{nd} December 2015 – 08:30 to 12:20hrs.

Fan-out WLP – Innovative Packaging Solutions with Scalability

Yoon Seung Wook, PhD  
STATS ChipPAC, Singapore

Course Content

FO-WLP technologies have been in high volume manufacturing for over 7 years. FO-WLP has matured enough that it has come to a crossroads where it has the potential to change the electronic packaging industry by eliminating traditional flip chip or wirebond assembly technologies across multiple applications. Market analysts are expecting a growth of 30% per year for the next 5 years.

This course will give an overview of the FO-WLP technology, the market drivers, end applications, benefits and challenges facing industry-wide adoption will be discussed. Typical FO-WLP configurations will be reviewed in terms of their construction, manufacturing processes, materials and equipment, and electrical and thermal performance, together with package and board level reliability. Since the technology marks the convergence of fab, assembly, and test, the discussion will address questions on business model and technology challenges such as:
- Will it be applicable and cost-effective for complex devices such as ASICs and Microprocessors for mobile applications?
- Are the current standards for design rules, outline, and reliability applicable?
- Future trends of scalability: low cost solutions with panel approach
- Extensions to higher pin count packages and other arenas such as Digital, RF, automotive and MEMS sensors will be reviewed. Future trends will also be covered such as enhanced solder joint reliability, large die size, thin and ultra-thin packages, RDL (redistribution layer), 2.5D/3D FO-WLP, MCP (Multi Chip Package), FO-WLP, embedded components etc.

Course Outline:

1. FO-WLP trends
2. Migration toward FO-WLP processing
3. FO-WLP categories
4. Barriers and challenges: technology and business model
5. Test Approach: component level or wafer level final test
6. Case study: FO-WLP for WE/mobile/consumer/automotive applications (process, assembly flows, selection criteria, recent developments, and reliability)
7. Technology Innovation of FO-WLP: ultra-thin, integration, discrete embedded, 2.5D/3D and large scale carriers.
8. Future of FO-WLP

8. Conclusions

9. References

About the Course Leader

Dr. Yoon is currently in charge of Advanced Products & Technology Marketing in STATS CHIPPAC LTD. His major interests are for advanced wafer level products including eWLB/Fanout WLP, WLCSP, IPD, flipchip bumping, TSV (Through Silicon Via) technology and integrated SiP/module packaging. Prior to joining STATS CHIPPAC LTD, He was deputy lab director of MMC (Microsystem, Module and Components) lab, IME (Institute of Microelectronics), A*STAR, Singapore. “YOON” received Ph.D degree in Materials Science and Engineering from KAIST, Korea. He also holds MBA degree from Nanyang Business School, Singapore. He has over 200 journal papers, conference papers and trade journal papers, and over 25 US patents on microelectronic materials and electronic packaging.
Modeling and Design Solutions to Overcome Warpage Challenge for Fan-Out Wafer Level Packaging (FO-WLP) Technology

Dr. Che Faxing
IME, A-Star

Technical Session: 3rd December 2015, 16:20hrs
Venue: Pisces & Aquarius
Speaker Code in advanced programme: IP.3

Abstract

Electronic packaging technology has been evolving vast fast recently, such as 3D integrated circuit (IC) packaging with through silicon-via (TSV), 3D system in package (SiP), 2.5D with TSV interposer (TSI), package-on-package (POP), wafer-level chip scale packaging (WLCSP), fan-out wafer-level-packaging (FO-WLP), and so on. Among the advanced packaging technologies, FO-WLP technology gets more and more significant attention with its advantages of high-integration capability, small form factor, higher I/O density, cost effective and high performance for wide range application, such as networking, smartphone, tablet etc. Today, the market growth for FO-WLP is increasing strongly. One of the key factors driving this is the arrival of 2nd generation FO-WLP technology which enables multiple chips to be integrated on a single package with more redistribution layers (RDLs). There are two categories of FO-WLP process, one is the traditional wafer-like process and the other is substrate-like process called panel FO-WLP. In this study, we focused on the traditional wafer-like process with 12” wafer size.

So far, FO-WLP package technology is still facing lots of challenges, such as wafer warpage, die shift, and die protrusion. Among challenges, wafer warpage is one critical issue which is needed to be addressed for successful subsequent processes. In this study, methodology to reduce wafer warpage at different processes was proposed in terms of geometry design, material selection, and process optimization. The used package size is 15mm × 15mm including 2 chips with 8mm × 9mm and 2mm × 3mm chip size. The final package thickness is 200µm with both side RDL structures. Finite element analysis (FEA) of FO-WLP wafer process can lead to the possibility for virtual experiment, leading to an improved knowledge of how parameters influence the wafer process induced warpage. Recently, the wafer warpage was studied by researchers through numerical simulation and experimental methods to optimize structure design and material selection. However, most of simulation work focused on molding process without modeling whole wafer processes. In this study, wafer process modeling methodology was established considering process condition step by step including molding, RDL fabrication, wafer support system, molded wafer back grinding, back side RDL and wafer debonding processes. First of all, process modeling results were validated by experimental measurement data. The following parameters were simulated and design solutions were provided for reducing wafer warpage: ratio of die to molding thickness, ratio of die area to package area, die arrangement in package, molding compound material properties of Young’s modulus, CTE and Tg, molding temperature, support wafer material and thickness, dielectric material and thickness, Cu RDL area percentage. It was found that the following parameters are critical ones affecting warpage during processes: thickness ratio of die to mold, molding compound
and support wafer materials, dielectric material and RDL design. The detailed methodology and results will be presented in the paper. Some useful modeling results were recommended to process and design engineers to optimize design, material selection and process conditions for reducing wafer warpage during whole processes.

**About the author**

Faxing CHE received the Ph.D. degree in engineering mechanics from Nanyang Technological University, Singapore. He is currently a Scientist with the Institute of Microelectronics (IME), A*STAR, Singapore. His major research interests are design for reliability in fan out wafer-level packaging, 3-D advanced packaging integration with TSV technology, Cu wire bonding, finite-element modeling and simulation, and characterization of microelectronic packaging materials.

Prior to joining IME, he was a Senior Engineer with the United Test and Assembly Centre and STMicroelectronics, and a Staff Engineer with Infineon Technologies Asia Pacific, Singapore. He has authored and co-authored over 100 technical papers in refereed journals and conference proceedings. Dr. Che serves as a peer reviewer for more than 10 international scientific journals. He was a recipient of the Best Poster Paper Award from the EPTC in 2013, the Best Poster Paper Award from ITherm in 2006, the Best Paper Award from the ICEPT in 2006, and the Outstanding Student Paper Award from the EPTC in 2003.
Abstract

New and emerging applications in the consumer and mobile space, the growing impact of the Internet of Things (IoT) and wearable electronics, and the slowdown of Moore's law have been driving many new trends and innovations in advanced packaging technology. The semiconductor industry now has to focus on integration and system scaling to meet the ever-increasing electronic system demands for performance and functionality as well as the reduction of form factor, power consumption and cost. This paradigm shift from chip-scaling to system-scaling will re-invent microelectronics packaging, continue driving system bandwidth and performance, and help sustain Moore’s Law. It also drives overall demand for maximum functional integration in the smallest and thinnest package with the lowest cost. The challenge for the semiconductor industry is to develop a disruptive packaging technology platform capable of achieving these goals. The most promising solutions in volume production today are Fan-out Wafer Level Packaging (FOWLP) such as embedded Wafer Level Ball Grid Array (eWLB) which provides significant bandwidth, performance, form factor and cost benefits compared to other packaging technologies available today.

This article will discuss the wide range of FOWLP/eWLB adoptions and new features available for mobile, IoT and wearable applications. This advanced technology is well designed for MEMS/sensors, 3D SiP modules as well as thin, highly integrated packaging solutions. Innovative FOWLP/eWLB features will be also introduced with the merits and characterization data for specific applications...

About the author

Dr. YOON is currently in charge of Advanced Products & Technology Marketing in STATS CHIPPAC LTD. His major interests are for wafer level products including TSV (Through Silicon Via) technology, eWLB/Fanout WLP, WLCSP, IPD, bumping, flipchip and integrated SiP/module packaging.

Prior to joining STATS CHIPPAC LTD, He was deputy lab director of MMC (Microsystem, Module and Components) lab, IME (Institute of Microelectronics), A*STAR, Singapore. “YOON” received Ph.D degree in Materials Science and Engineering from KAIST, Korea. He also holds MBA degree from Nanyang Business School, Singapore. He has over 200 journal papers, conference papers and trade journal papers, and over 25 US patents on microelectronic materials and electronic packaging.
Abstract
For emerging applications requiring significantly higher performance and bandwidth, a transition from fan-in WLCSP to fanout wafer level packaging (FO-WLP) is required to achieve maximum connection density, improved electrical and thermal performance and small package dimensions. FO-WLP, also known as embedded Wafer Level Ball Grid Array (eWLB), is an interconnection system processed directly on the wafer and is compatible with motherboard technology pitch requirements.

As demonstrated by witnessed by the dramatic evolution of cellular phones, product differentiation today is driven by ever-expanding functionality, feature sets, and faster communications. At the same time, consumers have made clear their desires for feature-rich products in compact form factors to enable maximum portability. eWLB technology is successfully enabling semiconductor manufacturers to provide the smallest possible and the highest performing semiconductors. Currently eWLB devices are used in baseband processors, RF transceivers, connectivity, near field communication (NFC), security devices, microcontrollers (MCU), memory, memory controllers, RF-MEMS and power management ICs. There has been a steady customer adoption and added opportunities such as MEMS, fingerprint sensors and wearable electronics. eWLB devices are found in all leading mobile products as well as in consumer electronics.

At present, the primary high volume ICs are baseband, RF Transceiver, power management integrated circuits (PMIC), power controller, NAND memory controller, connectivity, and security devices. Accelerated near-term customer adoption is taking place in logic processors, RF, audio and connectivity devices, 77GHz ADAS automotive devices, and MEMS/sensor devices. eWLB solutions are now in high volume production on 28 nm Si node and starting to ramp 20 nm devices.

In a number of cases, eWLB achieved a 20~40% reduction in package size as compared to other packaging solutions and over 50% volume reduction due to its slim and smaller form factor. For RF and high frequency devices, eWLB showed less parasitic electrical performance thus it also significantly improved overall device performance. eWLB technology is an important complementary solution to standard WLPs, enabling the next generation of a mobile, IoT (Internet of Things) and wearable applications. The benefits of standard fan-in WLPs such as low packaging/assembly cost, minimum dimensions and height as well as excellent electrical and thermal performance are equally true for eWLB as well. The ability to integrate passives like inductors, resistors and capacitors into the various thin film layers, active/passive devices into the mold compound and 3D vertical interconnection opens additional design possibilities for new Systems-in-Package (SIP) and 2.5D/3D packaging. Moreover, next generation, SiP-eWLB/3D eWLB technology provides more value-add in performance and promises to be
the new packaging platform that can expand eWLB application range to various types of devices for true 3D SiP/module systems.

This paper will present FO-WLP/eWLB technology introduction with competitive features, current applications and market attraction. Also discuss for future applications of 2.5D/3D eWLB for highly integrated solutions, such as MEMS/sensor and 3D moldue/SiP.

About the author

Dr. YOON is currently in charge of Advanced Products & Technology Marketing in STATS CHIPPAC LTD. His major interests are for wafer level products including TSV (Through Silicon Via) technology, eWLB/Fanout WLP, WLCSP, IPD, bumping, flipchip and integrated SiP/module packaging.

Prior to joining STATS CHIPPAC LTD, He was deputy lab director of MMC (Microsystem, Module and Components) lab, IME (Institute of Microelectronics), A*STAR, Singapore. “YOON” received Ph.D degree in Materials Science and Engineering from KAIST, Korea. He also holds MBA degree from Nanyang Business School, Singapore. He has over 200 journal papers, conference papers and trade journal papers, and over 25 US patents on microelectronic materials and electronic packaging.
Wafer Level Chip Size Package by using Post Dicing Process and its Application to the CMOS Image Sensor Module for Medical Device

Dr. Noriyuki Gujimori
Olympus Corp

Abstract
Recently, medical electronic devices demand various kind of electronic package. And the WL-CSP is one of most attractive technology for the in-vivo medical device applications in order to realize its minimal invasiveness. However, in the case of small amount of production quantity for the medical electronic devices, it causes an increase of the packaging cost if the large-wafer based packaging is utilized. In this study, a new packaging technique has been realized and applied to the imaging module for medical endoscope. In this new technique, the CMOS image sensor wafer is diced and then individual image sensor chips are rearranged on another smaller handling wafer. As the result, arbitrary size of handling wafer can be selected, and the rearranged WL-CSP leads to results in lower cost and shorter production lead-time

About the author
Noriyuki Fujimori is a manager of image sensor package and medical imaging technology development division. He graduated from Meiji University in the mechanical engineering department in 1997, and joined MEMS development group of Olympus in 1997 for Bio/Medical MEMS R&D. He has experience of developing swallowable capsule endoscope.
High Density Package Integration for Wearables and IoT Applications by eWLB based WLSiP and WLPoP

Steffen Kröhnert
NANIUM S.A., Director of Technology

Technical Session: 4th December 2015, 10:40hrs
Venue: Taurus
Speaker Code in advanced programme: IS.6

Abstract
The next big wave, the Internet of Things or Internet of Everything (IoT/IoE) is on the way. What does that mean for semiconductor packaging, assembly and test? What are the requirements? Which solutions can be provided? The market will be wide and fragmented. Many different solutions will be needed. Flexibility and the capability to customize system solutions will be crucial. Fact is, it will be all about smart system integration, integration of Sensors, MEMS, Connectivity and Memory: More functionality on less space in small and thin SiP and PoP. There will not be one specific packaging technology for IoT/IoE, and no new “IoT/IoE Packaging Technology”. The toolbox is here already, and further features required to meet the needs of future IoT/IoE modules are under development already. That is actually good news, as the cost pressure will be high, and materialization of existing manufacturing environment, of mature and yielding packaging technologies will be a key for success.
The paper will present latest development status of Fan-Out Wafer-Level Packaging (FOWLP), which are enabling IoT/IoE solutions, namely in the segment of wearable electronics, which seems to be the most advanced area of the IoT/IoE. The FOWLP technology eWLB (embedded Wafer-Level BGA) allows highest integration density in 2D, and is further developing to very thin 3D solutions right now. First constructions with embedded actives, discrete passives, already packaged dies and optical elements, qualified and getting ready for volume production will be presented including reliability results. Thin reconstituted wafer handling, thru package via and backside thin-film RDL processing solutions as enabler for thin eWLB based PoP will be discussed.

About the author
Dipl.-Ing. Steffen Kröhnert received his master degree in Electrical Engineering and Microsystem Technology at Technical University of Chemnitz, Germany, in 1997. In the same year he started his professional career as Development Engineer in the Corporate Package Assembly, Interconnect and Test Development Center for Semiconductors of Siemens AG in Regensburg, Germany. After carve out of the Semiconductors Business Unit to Infineon Technologies AG in 1999, he worked as Project Manager and moved to Infineon Dresden GmbH & Co. OHG in 2002 to support local setup of Package Development Department for Memory Products. He became R&D Area Manager Component Development and took over Technology Platform ownership for FBGA products. From 2006 he was working as Senior Manager in Qimonda Dresden GmbH & Co. OHG, the carve out of the Memory Products Business Unit of Infineon Technologies. Begin of 2007 he was assigned to Qimonda Portugal S.A., the largest Packaging, Assembly and Test facility of Qimonda, in order to setup and lead the Package Development team at this volume production site. Since 2009 he is Director of Technology at NANIUM S.A. in Vila do Conde, Portugal, the largest independent Semiconductor Packaging, Assembly and Test Foundry (OSAT) in Europe. Steffen is author and co-author of 23 patent filings in the area of Semiconductor Packaging Technology. He is member of IEEE CPMT, IMAPS, MEPTEC, SMTA, VDI, VDE and GPM. He actively contributes as Co-Chair
to SEMI Europe’s Advanced Packaging Conference (APC), as Technical Committee member to IEEE Electronic Components and Technology Conference (ECTC), IEEE Electronics System-Integration Technology Conference (ESTC) and IMAPS European Microelectronics Packaging Conference (EMPC), and as Assistant Technical Co-Chair (Europe) to IMAPS Device Packaging Conference and International Symposium on Microelectronics.
Abstract

Increasingly WLCSP are used as low cost solution for packaging, especially when the area needed for I/O matches the area needed for the function. Industry trend is to go thinner devices and smaller pitches. The mechanical integrity of WLCSP’s is stressed not only in the application, but also during assembly.

The breakthrough technology presented provides protection for all 6 sides of the product. The challenges experienced to create the fully encapsulated concept as well as the impact on die stress and Board Level Reliability will be shown. Different material sets and molding technologies to do encapsulation of the WLCSP were investigated, each with their own merits.

The encapsulation concept to achieve full encapsulation is demonstrated on a lab scale a true industrial solution is under development. By balancing the front and back side thickness of the compound it is possible to reduce the overall height and at the same time improving the BLR performance compared to more conventional 5 side protected WLCSP.

Biography

Tonny Kamphuis received his master in Mechanical Engineering at Twente University in 1986. The same year he joined Philips Semiconductors in the field of IC assembly equipment. He worked in Kaohsiung Taiwan from 1991 to 1992, after which he joined the discrete assembly equipment development department in Nijmegen. He has developed die bonders, wire bonders, molding machines as well as all type of handling equipment for both reel to reel and strip to strip based industrializations. Since the year 2000 he is focusing on assembly process development and industrialization for IC again. In 2007 NXP was founded, at NXP, he has filed several patents related to wafer processing, package concepts and process improvements.
Abstract

The wafer-level package (WLP) continues to see strong growth driven by mobile phones, tablets, portable players, wearable and IOT devices with its benefits of small form factor and low profile packages. Besides a wafer level chip scale package (WLCSP) as it fits the requirements, within the last few years, more and more talks for WLCSP packages to increase I/O density and performance into applications with higher levels of complexity.

The packaging subcons, have developed the need for an evolution in functionality of WLP technology and are just now beginning to put those processing capabilities to broader use. In this section, we will review a wide variety of wafer level processing technologies and packaging structures with higher levels of integration.

Basically to improving the conventional WLCSP structure to keep the side wall crack issue away from assembly process, we would like to introduce a Mold Type WLCSP (mWLCSP) to provide five sided protection for the exposed silicon in a WLCSP.

Wafer Level Fan-out (FOWLP) as a platform of embedded technology is considered a solution to achieve higher IO routing on the additional space of molding compound and extend the package size which is not possible in conventional WLCSP. Also, 3D structure of Package-on-Package (PoP) with double side integration which helping numerous active or passive components embedded inside in potable driven applications has been well developed as well.

Moreover, we will have a closer look on a cost down solution – No TSV Interposer (NTI) to compete with 2.5/3D technologies which requiring higher cost TSV based.

The incoming wafer for NTI is a very fine line (<2um L/S) wafer and it can provide the initial high density and split die interconnection with advanced silicon node.

Biography

Education:
Master of mechanical engineering department, Univ. of Chung-Hsing, Taiwan

Job Experience:
Over 18 years of job experience on semiconductor industry, especially focus on wire bond and flip chip advanced assembly technology
Now:
Deputy Director of Customer Advanced Product Division of SPIL (Siliconware, Taiwan), which is 3rd biggest assembly house in the world now