REGISTRATION IS NOW OPEN

EPTC 2017 Registration details can be found here

The 19th Electronics Packaging Technology Conference (EPTC 2017) is an International event organized by the IEEE Reliability/CPMT/ED Singapore Chapter and sponsored by IEEE CPMT Society. EPTC 2017 will feature technical sessions, professional development courses, forums, an exhibition, social and networking activities.

PROFESSIONAL DEVELOPMENT COURSES

The conference program includes short courses (6 Dec 2017), which will be conducted by leading experts in the field.

- Dr. Rick Sturdivant (Azusa Pacific University, USA), "Electronic Packaging for 5G Microwave and Millimeter Wave Systems"
- Dr. Mervi Paulasto-Kröckel (Aalto University, Finland), "small volume interconnect reliability and failure mechanisms for power/automotive package"
- Dr. Liu Aiqun (NTU), "MEMS Fabrication and Packaging"
- Dr. John H Lau (ASM), Fan-Out Wafer-Level Packaging and 3D Packaging
- Dr. Stevan Hunter (On Semiconductor), "Reliability from a Semiconductor Suppliers Perspective"
- Dr. Shi-Wei Ricky Lee (Hong Kong University of Science & Technology), "LED packaging technology and reliability"

PDC details can be found here

KEYNOTE SPEAKERS

- Dr. Wai Kooi Wong, Vice President, Quality And Reliability, Xilinx, "Extending Moore's Law with Advanced Packages"
- Dr. Rajendra Pendse, Senior Direcor, Packaging Stratagy, Qualcomm, "The Evolution of Packaging Technology for Mobile Platforms – Where We have been and where we are headed"
- Prof. C Bailey, Director of the Computational Mechanics and Reliability Group, University of Greenwich, "Design tools and modelling for power electronics packages – current status and future challenges"

Invited Speakers

- Mr. Albert Lan, Global Packaging TD, Applied Materials, "Innovative Process and Equipment Technology Solutions for 3D SiP Packaging"
- Prof. Avram Bar-Cohen, Principal Engineering Fellow, Raytheon Corporation, "On-Chip Embedded Cooling of Power and Logic Components"
- Dr. Kenzo Ohkita, Manager, JSR Corporation, "UV Laser Releasable Temporary Bonding Materials for Advanced Packaging technologies"
- Mr. Eric Pabo, Business Development Manager for MEMS, EV Group, "Wafer Bonding – An Enabling Technology for 3DIC, MEMS, BSI CIS, SOI, RF Filters, and More"

- Ram Trichur, Director of Business Development, Brewer Science, "Temporary Bonding Materials for Fan-out Packaging Processes"
- Dr. Stevan G. Hunter, MTS, On Semiconductor, "Reliability Assurance: A Semiconductor Supplier's Perspective"
- Dr. Yasuhiro Morikawa, Manager, Ulvac, "Highly accurate TSV, PWB and FO-PLP wirring fabication by plasma dry processes for interface"
- Dr. Hideyuki Nasu, Furukawa Electric Co., Ltd., "VCSEL-based Optical Interconnects and Their Packaging Technologies"
- Dr. Junsu Lee, Senior Packaging Scientist, Tyndall Research Institute, "Packaging of Integrated Silicon Photonic devices: Electrical, Optical, Thermal Challenges and Applications"
- Dr Napetschnig, Senior Staff Engineer, Infineon, "10 Golden Rules of Chip-Package- Board Interactions"
- Dr. Seung Wook Yoon, Director, Business Development, STATSChipPac Pte, Ltd., "Advanced eWLB FOWLP: Enabling Integrated Packaging Solutions"
- Dr. Guilian Gao, Xperi, "Enhanced Bonding Technology for Hybrid Integration in 3D Packaging Technology"

PANEL TOPIC HIGHLIGHTS

PANEL SESSION ON "Challenge of 5G-mm Wave Packaging & Opportunity" moderator - Dr. Rick Sturdivant, Department of Engineering and Computer Science, Azusa Pacific University, USA.

CONFERENCE TOPICS

- Advanced Packaging: advanced flip-chip, 2.5D & 3D, PoP, embedded passives & actives on substrates, System in Package, embedded chip packaging technologies, panel level packaging, RF, Microwave & Millimeter-wave, power and Rugged Electronics Packaging etc.
- TSV/Wafer Level Packaging: wafer level packaging (Fan In/Fan Out), embedded chip packaging, 2.5D/3D integration, TSV, silicon & glass interposers, RDL, bumping technologies, etc.
- Interconnection Technologies: Au/Ag/Cu/Al wire-bond / wedge bond technology, flip-chip & Cu pillar, solder alternatives (ICP, ACP, ACF, NCP, ICA), Cu to Cu, wafer level bonding & die attachment (Pb-free) etc.
- Emerging Technologies: packaging technologies for MEMS, biomedical, optoelectronics, internet of things, photovoltaic, printed electronics, wearable electronics, photonics, LED, etc.
- Materials and Processing: advanced materials, 3D materials, photoresists, polymer dielectrics, solder materials, die attach, underfill, substrates, leadframes, PCB etc for advanced packaging, and assembly processes using advanced materials, etc.
- Equipment and Process Automation: new processes development, equipment automation, equipment hardware development/improvements, data analytics, in-situ metrology, etc.
- Electrical Simulations & Characterization: Power plane modeling, signal integrity analysis of package. 2D/2.5D/3D package level high-speed signal design, characterization and test methodologies, etc.
- Mechanical Modeling & Simulations: thermo-mechanical, moisture, fracture, fatigue, vibration, shock and drop impact modeling, chip-package interaction, reliability, virtual prototyping, etc.
- Thermal Characterization & Cooling Solutions: thermal modeling and simulation, component, system and product level thermal management and characterization.
- Quality, Reliability & Failure Analysis: component, board, system and product level reliability assessment, interfacial adhesion, accelerated testing, failure characterization, etc.

Zhang Xueren, *General Chair*
Vempati Srinivasa Rao, *Technical Chair*

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