Conference Agenda

19th Electronics Packaging Technology Conference

Date: Wednesday, 06/Dec/2017			
7:00am - 8:30am	**PDC Registration**		
8:30am - 12:00pm	***PDC 1: Electronic Packaging for 5G Microwave and Millimeter Wave Systems IEEE by Dr. Rick Sturdivant*** Location: **Paradiso Room**	***PDC 2: Automotive electronics – requirements and reliability by Dr. Mervi Paulasto-Kröckel*** Location: **Cardinal Room**	***PDC 3: MEMS Fabrication: from theory to packaging by Dr. Liu Aiqun*** Location: **Swallow Room**
12:00pm - 1:30pm	**Lunch**		
1:30pm - 5:00pm	***PDC 4: Fan-Out Wafer-Level Packaging and 3D Packaging by Dr. John H Lau*** Location: **Paradiso Room**	***PDC 5: Reliability from a Semiconductor Suppliers Perspective by Dr. Stevan Hunter*** Location: **Cardinal Room**	***PDC 6: Advanced LED packaging technology and reliability by Dr. Ricky Lee*** Location: **Swallow Room**
5:30pm - 7:30pm	***Panel: Panel Session : Challenge of 5G-mm Wave Packaging & Opportunity*** Location: **Galleria Ballroom**		
7:30pm - 10:00pm	**Dinner: VIP**		

Date: Thursday, 07/Dec/2017					
7:45am - 8:30am	Conference Day 1 Registration				
8:30am - 9:00am	**Opening: Welcome and opening speech** Location: **Grand Ballroom**				
9:00am - 9:30am	***Keynote speech 1: Extending Moore's Law with Advanced Packages by W.K.Wong(Xilinx)***				
9:30am - 10:00am	***Keynote speech 2: : The evolution of packaging technology for mobile platform - Where we have been and where we are headed by Dr. Raj Pendse(Qualcomm)***				
10:00am - 10:30am	**Coffee/Tea Breaks #1: Interactive session #1**				
10:30am - 12:10pm	*A-01: ID 283*	*A-02: ID 169*	*A-03: ID 127*	*A-04: ID 119*	*A-05: ID 109*
	A-06: ID 190	*A-07: ID 203*	*A-08: ID 207*	*A-09: ID 125*	*A-10: ID 113*
	A-11: ID 256	*A-12: ID 246*	*A-13: ID 191*	*A-14: ID 137*	*A-15: ID 123*
	A-16: ID 300	*A-17: ID 205*	*A-18: ID 140*	*A-19: ID 167*	*A-20: ID 142*
	A-21: ID 174	*A-22: ID 110*	*A-23: ID 128*	*A-24: ID 188*	*A-25: ID 154*
	S-01: TSV/Wafer Level Packaging Location: **Paradiso Room**	**S-02: Interconnection Technologies** Location: **Cardinal Room**	**S-03: Material and Processing** Location: **Swallow Room**	**S-04: Mechanical modeling & simulation** Location: **Lyrebird Room**	**S-05: Quality, Reliability & FA** Location: **Falcon Room**
12:10pm - 1:30pm	**Lunch 01: Luncheon Talk, Presentation of EPTC 2016 Best Paper Awards, Presentation of IEEE CPMT Certification of Appreciation to EPTC 2017 Organizing Committee** Location: **Grand Ballroom**				
1:30pm - 2:00pm	***Invited-01: Enhanced Bonding Technology for Hybrid Integration in 3D Packaging Technology : Dr. Guilian Gao(Xperi)*** Location: **Paradiso Room**	***Invited-02: Packaging of Integrated Silicon Photonics devices : Electrical, Optical, Thermal Challenges and Application : Dr. Jun Su Lee(Tyndall National Institute)*** Location: **Cardinal Room**	***Invited-03: Innovative Process and Equipment Technology Solutions for 3D SiP Packaging : Albert Lan(Applied Material)*** Location: **Swallow Room**	***Invited-04: UV Laser Releasable Temporary Bonding Materials for Advanced Packaging technologies : Dr. Kenzo Ohkita(JSR)*** Location: **Lyrebird Room**	**Invited-05: To be updated** Location: **Falcon Room**
2:00pm - 3:20pm	*B-01: ID 286*	*B-02: ID 121*	*B-03: ID 172*	*B-04: ID 175*	*B-05: ID 237*
	B-06: ID 204	*B-07: ID 282*	*B-08: ID 206*	*B-09: ID 296*	*B-10: ID 208*
	B-11: ID 280	*B-12: ID 141*	*B-13: ID 220*	*B-14: ID 231*	*B-15: ID 224*
	B-16: ID 294	*B-17: ID 185*	*B-18*	*B-19: ID 166*	*B-20: ID 144*
	S-06: Advanced packaging Location: **Paradiso Room**	**S-07: Emerging Technologies** Location: **Cardinal Room**	**S-08: Equipment and Process automation** Location: **Swallow Room**	**S-09: Material and Processing** Location: **Lyrebird Room**	**S-10: Interconnection Technologies** Location: **Falcon Room**
3:20pm -	**Coffee/Tea Breaks #2: : Exhibitor Presentation**				

4:40pm					
4:40pm - 6:00pm	***C-01: ID 193***	***C-02: ID 163***	***C-03: ID 112***	***C-04: ID 122***	***C-05: ID 126***
	C-06: ID 194	***C-07: ID 164***	***C-08: ID 134***	***C-09: ID 162***	***C-10: ID 130***
	C-11: ID 201	***C-12: ID 165***	***C-13: ID 135***	***C-14: ID 108***	***C-15: ID 146***
	C-16: ID 216	***C-17: ID 197***	***C-18: ID 155***	***C-19: ID 213***	***C-20: ID 180***
	S-11: Mechanical modeling & simulation Location: **Paradiso Room**	**S-12: Quality, Reliability & FA** Location: **Cardinal Room**	**S-13: Thermal Characterization & cooling solutions** Location: **Swallow Room**	**S-14: Emerging Technologies** Location: **Lyrebird Room**	**S-15: Electrical Simulation & Characterization** Location: **Falcon Room**
6:30pm - 10:00pm	**Conference Banquet**				

Date: Friday, 08/Dec/2017					
8:30am - 9:00am	*Invited-06: Wafer Bonding – An Enabling Technology for 3DIC, MEMS, BSI CIS, SOI, RF Filters, and More : Eric Pabo(EVG)* Location: **Paradiso Room**	*Invited-07: VCSEL-based Optical Interconnects and Their Packaging Technologies : Dr. Hideyuki Nasu(Furukawa Electric Co)* Location: **Cardinal Room**	*Invited-08: Temporary Bonding Materials for Fan-out Packaging Processes : Ram Trichur(Brewer Science)* Location: **Swallow Room**	*Invited-09: On-Chip Embedded Cooling of Power and Logic Components : Dr. Avram Bar-Cohen(Raytheon Corporation)* Location: **Lyrebird Room**	*Invited-10: Reliability Assurance: A Semiconductor Supplier's Perspective : Dr. Stevan G. Hunter(ON Semiconductor)* Location: **Falcon Room**
9:00am - 10:20am	*D-01: ID 104*	*D-02: ID 170*	*D-03: ID 230*	*D-04: ID 171*	*D-05: ID 198*
	D-06: ID 266	*D-07: ID 288*	*D-08: ID 292*	*D-09: ID 173*	*D-10: ID 243*
	D-11: ID 305	*D-12: ID 214*	*D-13: ID 181*	*D-14: ID 192*	*D-15: ID 268*
	D-16: ID 281	*D-17: ID 298*	*D-18: ID 189*	*D-19: ID 265*	*D-20: ID 279*
	S-16: Interconnection Technologies Location: **Paradiso Room**	S-17: Emerging Technologies Location: **Cardinal Room**	S-18: Material and Processing Location: **Swallow Room**	S-19: Thermal Characterization & cooling solutions Location: **Lyrebird Room**	S-20: Quality, Reliability & FA Location: **Falcon Room**
10:20am - 11:00am	Coffee/Tea Breaks #3: Exhibitor Pressentation				
11:00am - 12:20pm	*E-01: ID 159*	*E-02: ID 272*	*E-03: ID 103*	*E-04: ID 186*	*E-05: ID 236*
	E-06: ID 153	*E-07: ID 116*	*E-08: ID 195*	*E-09: ID 196*	*E-10: ID 252*
	E-11: ID 124	*E-12: ID 222*	*E-13: ID 218*	*E-14: ID 211*	*E-15: ID 278*
	E-16: ID 254	*E-17: ID 143*	*E-18: ID 247*	*E-19: ID 228*	*E-20: ID 295*
	S-21: Materials and Processing Location: **Paradiso Room**	S-22: Advanced Packaging Location: **Cardinal Room**	S-23: TSV/Wafer Level Packaging Location: **Swallow Room**	S-24: Electrical Simulations & Characterization Location: **Lyrebird Room**	S-25: Mechanical Modeling & Simulations Location: **Falcon Room**
12:20pm - 1:20pm	Lunch 02: Presentation of Appreciation to Invited Papers' Authors, 19th Electronic Packaging Technology Conference Organisation Committee Appreciation, 20th Electronic Packaging Technology Conference Introduction Location: **Grand Ballroom**				
1:20pm - 1:50pm	*Invited-11: Advanced eWLB FOWLP: Enabling Integrated Packaging Solutions : Dr. Seung Wook Yoon(STATS ChipPAC)* Location: **Paradiso Room**	*Invited-12: Highly accurate TSV, PWB and FO-PLP wirring fabication by plasma dry processes for interface : Dr. Yasuhiro Morikawa(ULVAC)* Location: **Cardinal Room**	*Invited-13: 10 Golden Rules of Chip-Package- Board Interactions : Dr. E.Napetschnig(Infineon Technologies Austria)* Location: **Swallow Room**	*Invited-14: Update of Heterogeneous Integration Roadmap : William Chen, IEEE Electronic Packaging Society* Location: **Lyrebird Room**	
1:50pm - 3:10pm	*G-01: ID 151*	*G-02: ID 304*	*G-03: ID 120*	*G-04: ID 249*	*G-05: ID 233*
	G-06: ID 209	*G-07: ID 177*	*G-08: ID 105*	*G-09: ID 244*	*G-10: ID 245*
	G-11: ID 179	*G-12: ID 250*	*G-13: ID 217*	*G-14: ID 161*	*G-15: ID 270*
	G-16: ID 275	*G-17: ID 221*	*G-18: ID 114*	*G-19: ID 253*	
	S-26: Advanced	S-27: TSV/Wafer	S-28: Interconnection	S-29: Emerging	S-30: Electrical

	Packaging Location: **Paradiso Room**	Level Packaging Location: **Cardinal Room**	Technologies Location: **Swallow Room**	Technologies Location: **Lyrebird Room**	Simulations & Characterization Location: **Falcon Room**
3:10pm - 3:40pm	**Coffee/Tea Break #04: Interactive session #2**				
3:40pm - 4:10pm	***Keynote speech 3: Design tools and modelling for power electronics packages – current status and future challenges : Prof. Bailey(University of Greenwich)***				
4:10pm - 4:30pm	**Closing Ceremony: Lucky Draw**				

Date: Saturday, 09/Dec/2017

8:30am - 12:00pm	**Visit: Institution Visit**

ORAL Presentations

Advanced Packaging

E-07: ID 116

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 116 / E-07: 1
Advanced Packaging
Keywords: Chip on Wafer, Non-Conductive Film, Gang Bonding

Development of Chip on wafer Bonding with Non-Conductive Film using Gang Bonder

Ser Choong Chong, Hongyu Li, Ling Xie, Sekhar Vasarla Nagendra, Daniel Ismael Cereno
Institute Of Microelectronics, Singapore; chongsc@ime.a-star.edu.sg

E-17: ID 143

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 143 / E-17: 1
Advanced Packaging
Keywords: Footprint Design, System in Package, Large SMD

Solving Issues in a System-in-Package with Large SMD

Godfrey Cuevas Dimayuga, Jefferson Sismundo Talledo
ST Microelectronics, Philippines; godfrey.dimayuga@st.com

G-01: ID 151

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 151 / G-01: 1
Advanced Packaging
Keywords: Transformer, Power Amplifier, 802.11ac, CMOS, WLAN

Development of Highly efficient push-pull Power Amplifier with Center Tapped Transformer for 5GHz application

Tomoki Sadakiyo, Haruichi Kanaya
Kyushu University, Japan; 2IE16616G@s.kyushu-u.ac.jp

G-11: ID 179

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 179 / G-11: 1
Advanced Packaging
Keywords: Ultra thin WLCSP

Challenges of Ultra Thin WLCSP

Kelly Chen[1], Tom Tang[1], Mark Liao[1], Jensen Tsai[1], Steve Hsieh[2], Jerry Chang[2], Arthur Ho[2]
[1]SPIL, Taiwan; [2]NXP, Taiwan; kellychen@spil.com.tw

B-06: ID 204

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 204 / B-06: 1
Advanced Packaging
Keywords: Passive stress sensor, 28 nm node technology, Four-Point Bending

Passive Stress Sensor Development: From 65nm to 28nm Technology Nodes

Idir Raid[1], Rafael Estevez[2], Sébastien Gallois-Garreignot[1], Olivier Kermarrec[1]
[1]STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles Cedex, France; [2]SIMaP, Grenoble INP, CNRS UMR5266, 1130 rue de la Piscine, BP 75 38402 Saint Martin D'Hères, France; idir.raid@st.com

G-06: ID 209

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 209 / G-06: 1
Advanced Packaging
Keywords: GaN HEMT, Epoxy transfer, Transparent electronics and 3D Packaging

Gallium Nitride transistor on glass using epoxy mediated substrate transfer technology

Pavani Vamsi Krishna Nittala, Nayana Ramesh, Nagaboopathy Mohan, Rangarajan Muralidharan, Srinivasan Raghavan, Digbijoy N Nath, Prosenjit Sen
CeNSE, Indian Institute of Science, Bangalore; vamsinittala@gmail.com

E-12: ID 222

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 222 / E-12: 1
Advanced Packaging
Keywords: 3D IC; ubump; reliability; side wall reaction; solid state reaction; high temperature storage

Reaction competition in micro-bump and the influences on reliabilities

Yi-Ting Henry Chen, Raghu Chaware, Inderjit Singh, Ramasamy Anandan
Xilinx; ramasam@xilinx.com

E-02: ID 272

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 272 / E-02: 1
Advanced Packaging
Keywords: inteproser, 2.5D integration, SERDES, high speed memory

Heterogeneous interposer based integration of chips onto interposer to achieve high speed interfaces for ADC application

Andy Heinig, Michael Dittrich, Fabian Hopsch
Fraunhofer IIS/EAS, Germany; andy.heinig@eas.iis.fraunhofer.de

G-16: ID 275

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 275 / G-16: 1
Advanced Packaging
Keywords: wafer level packaging, vacuum, MEMS, Al-Ge bonding, eutectic

Wafer Level Vacuum Packaging with Al-Ge bonding for MEMS

Daw Don Cheam, Jae-Wung Lee, Bang Tao Chen, Navab Singh
Institute of Microelectronics, Singapore; leejw@ime.a-star.edu.sg

B-11: ID 280

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 280 / B-11: 1
Advanced Packaging
Keywords: Multi sensor, selective molding, Film Assist Molding, Dynamic Inserts

Selective over-molding of a CMOS TSV wafer with the flexible 3D integration of components and sensors

Johan Hamelink
Boschman Technologies, Netherlands; johanhamelink@boschman.nl

B-01: ID 286

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 286 / B-01: 1
Advanced Packaging
Keywords: Wafer Level Packaging, Fine Pitch RDL, Wafer Embedding, Neuromporphic Computing

Full Wafer Redistribution and Wafer Embedding as Key Technologies for a Multi-Scale Neuromorphic Hardware Cluster

Kai Zoschke[1], **Maurice Güttler**[2], **Lars Böttcher**[1], **Andreas Grübl**[2], **Dan Husmann**[2], **Johannes Schemmel**[2], **Karlheinz Meier**[2], **Oswin Ehrmann**[3]
[1]Fraunhofer IZM, Gustav-Meyer-Allee 25, 13355 Berlin, Germany; [2]Heidelberg University, Kirchhoff Institute for Physics, Im Neuenheimer Feld 227, 69120 Heidelberg; [3]Technical University of Berlin, Gustav-Meyer-Allee 25, 13355 Berlin, Germany; kai.zoschke@izm.fraunhofer.de

B-16: ID 294

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 294 / B-16: 1
Advanced Packaging
Keywords: Fanout technology, advanced wafer level packaging, multi chip module fanout packaging, reliability, yield, defectivity

Comprehensive Defect Monitoring Technique for Advanced Fanout Packaging Process

Vangal Aravindh[1], **Richard Yeoh**[1], **Wesley Chang**[2], **ShihLin Pan**[2], **Wei Kuo**[1], **Anuj Pandey**[1], **Kevin Khoo**[1], **Rahul Lakhawat**[1], **Kootz Wang**[1]
[1]KLA Tencor (1 Technology Dr, Milpitas, CA 95035, USA); [2]ASE (Lane 75, Waihuan West Road, Nanzi District, Kaohsiung City, Taiwan 811); Aravindh.Vangal@kla-tencor.com

TSV/Wafer Level Packaging

E-03: ID 103

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 103 / E-03: 1
TSV/Wafer Level Packaging
Keywords: Fan-Out Wafer Level Packaging, FO-SiP

Integration Benefits and Challenges on Fan-Out to Enable System in Package for IoT/Wearable Devices

Humi Tang[1], **Max Lu**[2], **Jensen Tsai**[3]
[1]Siliconware Precision Industries Co., Ltd. (SPIL), Taiwan; [2]Siliconware Precision Industries Co., Ltd. (SPIL), Taiwan; [3]Siliconware Precision Industries Co., Ltd. (SPIL), Taiwan; humitang@spil.com.tw

A-21: ID 174

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 174 / A-21: 1
TSV/Wafer Level Packaging
Keywords: Chip scale package, wafer-level packaging, wafer-level molding, TSV

Wafer-Level Packaging Technology for Optical Sensor Devices

Gregor Toschkoff, **Thomas Bodner**, **Harald Etschmaier**, **Franz Schrank**
ams AG, Austria; gregor.toschkoff@ams.com

G-07: ID 177

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 177 / G-07: 1
TSV/Wafer Level Packaging
Keywords: 3D stacking, TSV, stress, CMOS characteristic

Impact of 3D Stacking on the TSV-induced Stress and the CMOS Characteristics

Aki Dote, **Hiroko Tashiro**, **Hideki Kitada**, **Shinji Tadaki**, **Shoichi Miyahara**, **Seiki Sakuyama**
Fujitsu Ltd., Japan; dote.aki@jp.fujitsu.com

A-06: ID 190

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 190 / A-06: 1
TSV/Wafer Level Packaging
Keywords: TSV, Backside Via, DRIE

Novel ICP Plasma Etching for Backside TSV.

Toshiyuki Sakuishi, Takahide Murayama, Yasuhiro Morikawa
ULVAC,Inc., Japan; toshiyuki_sakuishi@ulvac.com

E-08: ID 195

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 195 / E-08: 1
TSV/Wafer Level Packaging
Keywords: Through-Silicon Via, BiCMOS, Heterogeneous Integration, Wafer Bonding

Through-Silicon Via Process Module with Backside Metallization and Redistribution Layer within a 130 nm SiGe BiCMOS Technology

Matthias Wietstruck[1], Steffen Marschmeyer[1], Marco Lisker[1], Andreas Krueger[1], Dirk Wolansky[1], Mirko Fraschke[1], Philipp Kulse[1], Alexander Goeritz[1], Mesut Inac[1,2], Thomas Voss[1], Andreas Mai[1], Mehmet Kaynak[1,3]
[1]IHP Microelectronics, Germany; [2]Technical University Berlin, Germany; [3]Sabanci University, Turkey; wietstruck@ihp-microelectronics.com

E-13: ID 218

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 218 / E-13: 1
TSV/Wafer Level Packaging
Keywords: WLP, pillar, electrodeposition, packaging, HDFO

Plating Challenges Associated with High-Density Fan-Out (HDFO) Technology

Kari Thorkelsson
Lam Research Corporation, United States of America; kari.thorkelsson@lamresearch.com

G-17: ID 221

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 221 / G-17: 1
TSV/Wafer Level Packaging
Keywords: large format packaging, encapsulant, dispensing strategies

Dispensing Challenges of Large Format Packaging and Some of Its Possible Solutions

Eric Teng Hock Kuah, Wei Ling Chan, Ji Yuan Hao, Chun Ho Fan, Ming Li, John Lau, Kai Wu
ASM Technology Singapore Pte Ltd, Singapore; eric.kuah@asmpt.com

E-18: ID 247

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 247 / E-18: 1
TSV/Wafer Level Packaging
Keywords: reconstituted wafer, fan-out, chip-first and die-up, redistribution layer, wafer level packaging.

Development of Chip-First and Die-Up Fan-out Wafer Level Packaging

Li Zhang[1], Dong Chen[1], Hong Xu[1], Xuan Hua[1], KH Tan[1], CM Lai[1], John Lau[2], Ming Li[2], Margie Li[2], Eric Kuah[2], Nelson Fan[2], Kai Wu[2], Ken Cheung[2]
[1]Jiangyin Changdian Advanced Packaging Co.,LTD; [2]ASM Pacific Technology; Tony_Chen@jcap.com.cn

G-12: ID 250

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 250 / G-12: 1
TSV/Wafer Level Packaging
Keywords: three-dimensional integrated circuit (3-D IC), power delivery, through silicon via (TSV), voltage drop

Effective Layout Scheme of Power and Ground TSVs for More Reliable Power Delivery in 3-D ICs

Weijun Zhu, Gang Dong, Zheng Mei
Xidian University, China, People's Republic of; mmzzkkxx@126.com

A-11: ID 256

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 256 / A-11: 1
TSV/Wafer Level Packaging
Keywords: Adhension, Backside dielectric, 2.5D/3D integration

The adhesion study of back-side dielectric film within 3D process integration

Hongyu Li
IME, Singapore; lihy@ime.a-star.edu.sg

A-01: ID 283

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 283 / A-01: 1
TSV/Wafer Level Packaging
Keywords: 3D technology, silicon interposer, TSV, power electronics, automotive, wafer level chip scale package, wafer level molding and balling, reliability

3D Si Interposer & WLP for Small Power Devices for Harsh Conditions

Jean Charbonnier[1], Aurélia Plihon[1], Myriam Assous[1], Maxime Argoud[1], Nacima Allouti[1], Stéphane Moreau[1], Nadine David[1], Catherine Brunet-Maquat[1], Christian Hartler[2], Joerg Siegert[2], Ewald Wachmann[2]
[1]CEA Leti, France; [2]ams AG, Austria; jean.charbonnier@cea.fr

A-16: ID 300

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 300 / A-16: 1
TSV/Wafer Level Packaging
Keywords: Fan-Out Wafer, Fan-Out Panel, RDL, PVD, Barrier - Seed

Carrier-Based Linear Transport PVD System Results for RDL Barrier/Seed Deposition in Fan-Out Packaging Applications

Paul Francis Werbaneth, Terry Bluck, Chun-Chung Chen, Daniel Gallagher, Vladimir Kudriavstev, Lisa Mandrell, Billy Runstadler, Chris Smith
Intevac, Inc., United States of America; pwerbaneth@intevac.com

G-02: ID 304

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 304 / G-02: 1
TSV/Wafer Level Packaging
Keywords: 2.5D/3D package, FO-WLP, PoP, eWLB, multi-chip

Enabling faster design and implementation decisions using virtual prototyping

Yoko Fujita
ZUKEN Inc., Japan; fujita.yoko@zuken.co.jp

Interconnection Technologies

D-01: ID 104

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 104 / D-01: 1
Interconnection Technologies
Keywords: Flip Chip, Thermal Compression Bonding, TCB, Coreless, Mass Reflow

Challenge and Warpage Optimization of Thermal Compression Bonding Technology on Coreless Substrates

Mike Tsai, Jensen Tsai, Yan Han Yao, Roger Lo, Cheng Kai Chang, Nicholas Kao
Siliconware Precision Industries Co. Ltd., Taiwan; miketsai@spil.com.tw

G-08: ID 105

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 105 / **G-08: 1**
Interconnection Technologies
Keywords: Three-Dimensional ICs, Through Silicon Via, TSV, NoC, CNT, Wireless, Optical, Microprocessor, NoC.

More than Moore and Beyond CMOS: New Interconnects Schemes and New Circuits Architectures

Khaled Salah Mohamed
Mentor, Egypt; khaled_mohamed@mentor.com

A-22: ID 110

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 110 / **A-22: 1**
Interconnection Technologies
Keywords: intermetallic compounds, solder, NiAu, fracture, interface

Revisiting brittle fracture in sandwiched solder system

Ian Harvey Arellano, Dexter delos Santos
STMicroelectronics, Inc., Philippines; ian-harvey.arellano@st.com

G-18: ID 114

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 114 / **G-18: 1**
Interconnection Technologies
Keywords: wire bonding, ag wire, silver wire, memory device, FEA model, wire bond looping, free air ball (FAB)

Optimizing Ag Wire Bonding for Memory Devices

Ivy Qin[1], Gary Schulze[1], Tom Rockey[1], Basil Milton[1], Bob Chylak[1], Nelson Wong[2]
[1]kulicke and soffa industries inc., United States of America; [2]kulicke and soffa Pte Ltd, Singapre; iqin@kns.com

G-03: ID 120

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 120 / **G-03: 1**
Interconnection Technologies
Keywords: Polyimide Flexible PCB, wirebonding

Challenges of Wirebonding with Polyimide Flexible Circuit Board(FPCB)

Norhanani Jaafar, Ramona Damalerio
Institute of Microelectronic, Singapore; jaafarn@ime.a-star.edu.sg

B-20: ID 144

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 144 / **B-20: 1**
Interconnection Technologies
Keywords: Pd distribution, Pd Cu wire, EFO condition, gas type, FAB

Effects of Pd distribution at free air ball in Pd coated Cu wire

Byung Hoon Jung[1,2], Byung Kwan Yu[1], Seung Hyun Kim[1], Jeong Tak Moon[1], Sang Jeen Hong[2]
[1]MK Electron Co. Ltd.,, Korea, Republic of (South Korea); [2]Myongji University, Cheoin-gu Yongin, Gyeonggo-do, (South Korea); bhjung@mke.co.kr

A-02: ID 169

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 169 / **A-02: 1**
Interconnection Technologies
Keywords: ultrasonic wire bonding, oxide removal process, real-time observation, bonding mechanism

Visualization of Oxide Removal during Ultrasonic Wire Bonding Process

Yangyang Long[1], Folke Dencker[2], Andreas Isaak[2], Friedrich Schneider[3], Jörg Hermsdorf[3], Marc Wurz[2], Jens Twiefel[1]
[1]Institute of Dynamics and Vibration Research, Leibniz Universität Hannover, Germany; [2]Institute of Micro Production Technology, Leibniz Universität Hannover, Germany; [3]Laser Zentrum Hannover e.V., Germany; long@ids.uni-hannover.de

A-07: ID 203

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 203 / A-07: 1

Interconnection Technologies

Keywords: Interconnects, 3D Integration, Fine Pitch, Flip Chip

Towards Reliable 10µm Pitch Assembly Using Cu/Ni/SnAg based Interconnects

Divya Taneja[1,2], Marion Volpert[1], Tarik Chaira[1], David Henry[1], Fiqiri Hodaj[2]

[1]CEA-LETI, France; [2]University Grenoble Alpes, SIMAP; divya.taneja@cea.fr

A-17: ID 205

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 205 / A-17: 1

Interconnection Technologies

Keywords: Silver Sintered Material, Automotive Power Devices, Lifetime Prediction, Manson-Coffin rule, ratchet phenomenon

Improvement of Lifetime Prediction of Silver Sintered Material in Automotive Power Devices

Ryosuke YAEJIMA[1], Shota OKUNO[1], Qiang YU[1], Yusuke NAKATA[2], Hiroyuki SUGAWARA[2]

[1]Yokohama National University, Japan; [2]Calsonic Kansei Co.,Ltd, Japan; yaejima-ryosuke-mn@ynu.jp

B-10: ID 208

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 208 / B-10: 1

Interconnection Technologies

Keywords: Cu-Cu bonding, low temperature, magnetron sputtering

Low Temperature Cu-Cu Bonding Using Tin Nanoparticles Fabricated by High Pressure Magnetron Sputtering

Zijian Wu[1], Qian Wang[1], Jian Cai[1,2]

[1]Institute of Microelectronics, Tsinghua University, Beijing, 100084, China; [2]Tsinghua National Laboratory for Information Science and Technology, Tsinghua University, Beijing, 100084, China; wu-zj12@mails.tsinghua.edu.cn

G-13: ID 217

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 217 / G-13: 1

Interconnection Technologies

Keywords: Ag wire bonding, intermetallic compound; biased-HAST

Challenges and feasibility of Ag wire bonding for Automotive Applications

Jing-en Luan

STMicroelectronics Pte Ltd, Singapore; jing-en.luan@st.com

B-15: ID 224

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 224 / B-15: 1

Interconnection Technologies

Keywords: copper wirebond, shear strength, reliability, intermetallic

Bond Pad Effects on Shear Strength of Copper Wire Bonds

Stevan G Hunter[1], Subramani Manoharan[2], Patrick McCluskey[2]

[1]ON Semiconductor, United States of America; [2]University of Maryland; sputterman0@gmail.com

B-05: ID 237

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 237 / **B-05: 1**
Interconnection Technologies
Keywords: die bonding, wire bonding, memory stacking, thin die, die crack

Leading Edge Die Stacking and Wire Bonding Technologies for Advanced 3D Memory Packages

Oranna Yauw[1], Andrew Tan[1], Aashish Shah[2], Jeong Ho Yang[1], Ivy Qin[2], Jie Wu[1], Gary Schulze[2]
[1]Kulicke & Soffa Pte. Ltd.; [2]Kulicke & Soffa Industries Inc.; wmoyauw@kns.com

A-12: ID 246

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 246 / **A-12: 1**
Interconnection Technologies
Keywords: Piezo Jet Printing, Power Electronics

Feasability Study of Piezo Jet Printed Silver Ink Structures for Interconnection and Condition Monitoring of Power Electronics Components

Martin Mueller, Joerg Franke
University Erlangen-Nuremberg, Germany; martin.mueller@faps.fau.de

D-06: ID 266

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 266 / **D-06: 1**
Interconnection Technologies
Keywords: Ultra-Fine-Pitch; Bonding; Dry film; Photolithography; Electroplating;

Ultra-Fine-Pitch Bonding Based On Photolithography And Electroplating

Dongyang Li[1], Xuhan Dai[2], Taegyu Kang[3], Guifu Ding[4]
[1]Department of Micro/Nano Electronics, Shanghaijiaotong University, China, People's Republic of; [2]Department of Micro/Nano Electronics, Shanghaijiaotong University, China, People's Republic of; [3]Samsung Electronics; [4]Department of Micro/Nano Electronics, Shanghaijiaotong University, China, People's Republic of; hildy7@163.com

D-16: ID 281

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 281 / **D-16: 1**
Interconnection Technologies
Keywords: bonding wire, ball bond, silver wire, stitch bond, free air ball

Novel Coated Silver (Ag) Bonding Wire: Bondability and Reliability

Senthilkumar Balasubramanian, Kang Il Tae, Lois Liao Jin Zhi, Evonne Evonne, Murali Sarangapani, Chee Wei Tok, James Kim Tae Yeop, Eric Tan Swee Seng, Xi Zhang
Heraeus Materials Singapore Pte Ltd, Singapore; senthilkumar.balasubramanian@heraeus.com

D-11: ID 305

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 305 / **D-11: 1**
Interconnection Technologies
Keywords: Die-attach, inkjet printing, NCA, adhesives

DIGITAL MICRO-DISPENSION OF NON-CONDUCTIVE ADHESIVES (NCA) BY INKJET PRINTER

Ali Roshanghias, Alfred Binder
CTR Carinthian Tech Research AG, Austria; ali.roshanghias@ctr.at

Emerging Technologies

C-14: ID 108

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 108 / C-14: 1
Emerging Technologies
Keywords: Paper electrode, dry transfer, Ag NP, Ag NW

Fabrication of paper electrode by dry transfer of Ag NP and Ag NW

Sunho Kim, Hoo-Jeong Lee
Sungkyunkwan University, Korea, Republic of (South Korea); sunhofy@skku.edu

B-02: ID 121

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 121 / B-02: 1
Emerging Technologies
Keywords: Silicon photonics, Optical MEMS switch, MEMS packaging, Glass interposer, Ion-exchanged waveguide

128 x 128 Silicon Photonics MEMS Switch Package using Glass Interposer and Pitch Reducing Fibre Array

How Yuan Hwang
Tyndall National Institute, Ireland; howyuan.hwang@tyndall.ie

C-04: ID 122

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 122 / C-04: 1
Emerging Technologies
Keywords: Sn immersion, failure mode, whiskers, mechanism, defect

Towards a deeper understanding of the failure modes in Sn immersion plating

Ian Harvey Arellano, Amor Zapanta
STMicroelectronics, Inc., Philippines; ian-harvey.arellano@st.com

B-12: ID 141

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 141 / B-12: 1
Emerging Technologies
Keywords: Compression Molding, MEMS-WLCSP, Silicon Pillars, Vertical Interconnections

Molding Process Development for Low-Cost MEMS-WLCSP with Silicon Pillars and Cu Wires as Vertical Interconnections

Mian Zhi Ding, Boon Long Lau, Zhaohui Chen
Institute of Microelectronics, Singapore; dingmz@ime.a-star.edu.sg

G-14: ID 161

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 161 / G-14: 1
Emerging Technologies
Keywords: NFC WISP, Wearable devices, coupling efficiency, flexible package

Design of NFC WISP system for wearable devices

Xuesong Zhang, Qian Wang, Han Guo, Yu Chen, Jian Cai
tsinghua university, China, People's Republic of; zhangxs15@mails.tsinghua.edu.cn

C-09: ID 162

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 162 / C-09: 1
Emerging Technologies
Keywords: Hermetic, Sealing, Packaging, Neural and biocompatible

Hybrid Hermetic Housings for Active Implantable Neural Device

CHENG Ming-Yuan, CHEN Weiguo, LIM Ruiqi, DAMALERIO Ramona
Institute of Microelectronics, A*STAR, Singapore; chengmy@ime.a-star.edu.sg

D-02: ID 170

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 170 / D-02: 1
Emerging Technologies
Keywords: printed electronics, direct metal printing, printed electrical connections, microdosage of molten metals

Direct printing of electrical connections from metal melts using StarJet technology

Michael Jehle[1], Björn Gerdes[1], Pavel Soukup[2], Michael Fechtig[1], Roland Zengerle[1], Peter Koltay[1], Lutz Riegger[1]
[1]University of Freiburg, Germany; [2]Advacam s.r.o.; michael.jehle@imtek.uni-freiburg.de

B-17: ID 185

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 185 / B-17: 1
Emerging Technologies
Keywords: EEG, ANSYS, sensor, PDMS, deformation

Simulation Analysis of a Wearable Dry EEG Electrodes for Epilepsy Monitoring

Weiguo CHEN[1], Ramona DAMALERIO[1], Ruiqi LIM[1], Yuan GAO[1], Derrick CHAN[2], Ming-Yuan CHENG[1]
[1]Institute of Microelectronics, Singapore; [2]KK Women's and Children's Hospital; chenwg@ime.a-star.edu.sg

C-19: ID 213

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 213 / C-19: 1
Emerging Technologies
Keywords: Microfluidics, surface roughness, wafer bonding, lab-on-chip, BiCMOS

Oxide Surface Roughness Optimization of BiCMOS BEOL Wafers for 200 mm Wafer Level Microfluidic Packaging Based on Fusion Bonding

Mesut Inac[1,2], Matthias Wietstruck[2], Alexander Göritz[2], Barbaros Cetindogan[2], Canan Baristiran-Kaynak[2], Marco Lisker[2], Andreas Krüger[2], Andreas Trusch[2], Ulrike Saarow[2], Patric Heinrich[2], Thomas Voss[2], Mehmet Kaynak[2,3]
[1]Technical University Berlin, Germany; [2]IHP, Frankfurt (Oder), Germany; [3]Sabanci University, Istanbul, Turkey; inac@tu-berlin.de

D-12: ID 214

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 214 / D-12: 1
Emerging Technologies
Keywords: Plasma Dicing, Endpoint Detection, Dicing After Grind

Novel End-Point Solution for Improvement in Die Strength and Yields with Plasma Dicing After Grind in Volume Production

Richard Barnett, Oliver Ansell, Martin Hanicenic, Janet Hopkins
SPTS Technologies Ltd, United Kingdom; richard.barnett@orbotech.com

G-09: ID 244

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 244 / G-09: 1
Emerging Technologies
Keywords: MEMS, MEMS Packaging, Pressure Sensor

Stress-Free Bonding Technology with Bondable Thin Glass layer for MEMS based Pressure Sensor

Ha-Duong Ngo[1,3], Xiaodong Hu[2,4], Oswin Ehrmann[2,3], Klaus-Dieter Lang[2,3], Martin Schneider-Ramelow[2,3], Ulli Hansen[4]
[1]University of Applied Sciences, Germany; [2]Technical University Berlin; [3]Fraunhofer Institut IZM; [4]MSG Lithoglas GmbH; hu@mat.ee.tu-berlin.de

G-04: ID 249

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 249 / **G-04: 1**
Emerging Technologies
Keywords: additive manufacturing, printed electronics, 3D integration, Aerosol Jet Printing (AJP), conductive silver tracks

Additive low temperature 3D printed electronic as enabling technology for IoT application

Serguei Stoukatch[1], Francois Dupont[1], Laurent Seronveaux[2], Denis Vandormael[2], Michael Kraft[1]
[1]University of Liege, Belgium; [2]Sirris, Belgium; serguei.stoukatch@ulg.ac.be

G-19: ID 253

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 253 / **G-19: 1**
Emerging Technologies
Keywords: graphene, carbon nanotubes (CNTs), three-dimensional integrated circuits (3D IC), through silicon vias (TSVs)

Growth and Fabrication of Carbon-Based Three-Dimensional Heterostructure in Through-Silicon Vias (TSVs) for 3D Interconnects

Ye Zhu, Chong Wei Tan, Shen Lin Chua, Yu Dian Lim, Beng Kang Tay, Chuan Seng Tan
Nanyang Technological University, Singapore; yzhu012@e.ntu.edu.sg

B-07: ID 282

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 282 / **B-07: 1**
Emerging Technologies
Keywords: Micro-Cooler, 3D-System-in-Package, Self-folding, RF communication, Micro-device

Ultra-Small Packaged Micro-Cooler for Medical Applications

José Miguel Fernandes[1], Pedro Anacleto[1], Luís Alexandre Rocha[1], João Gaspar[2], Paulo Mateus Mendes[1]
[1]Universidade do Minho, Portugal; [2]International Iberian Nanotechnology Laboratory; paulo.mendes@dei.uminho.pt

D-07: ID 288

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 288 / **D-07: 1**
Emerging Technologies
Keywords: Ag Nanoparticles, Ag nanoplates, low temperature

Ag Nanoparticles - Based Hybrid Ink with Low Metallization Temperature

Yongdian Han
Tianjin University, China, People's Republic of; hanyongdian@tju.edu.cn

D-17: ID 298

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 298 / **D-17: 1**
Emerging Technologies
Keywords: Printed Electronics, Werable Electronics

Evaluation of Printed Capacitive Touch Sensors for Touch Panel

W. FAN, B. K. LOK, F. K. LAI, J. WEI
SIMTech, Singapore; wfan@SIMTech.a-star.edu.sg

Materials and Processing

E-11: ID 124

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 124 / **E-11: 1**
Materials and Processing
Keywords: Envirnmental impact, Simapro Tool, X-Ray Fluorescence Analyzer, RoHS and WEEE

Environmental Impact Analysis Of Mi Band 2 Smart Wristband Watch Using Simapro Tools and X-Ray Fluorescence Analyzer (XRF)Technique

Man Man Ma
EPA Centre,City University of Hong Kong, Hong Kong S.A.R. (China); manmanma2-c@my.cityu.edu.hk

A-03: ID 127

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 127 / A-03: 1
Materials and Processing
Keywords: sintering silver paste, pressure assisted sintering, power cycling

The Correlation between Sintered Silver Joint Reliability and Pressure Assisted Sintering Parameters

Wayne Chee Weng Ng[1], Keith Sweatman[1], Kenji Takamura[1], Keisuke Kumagai[1], Takatoshi Nishimura[1], Sebastian Letz[2], Andreas Schletz[2]
[1]Nihon Superior Co., Ltd., Osaka, Japan; [2]Fraunhofer IISB, Nuremberg, Germany; wayne@nihonsuperior.co.jp

A-23: ID 128

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 128 / A-23: 1
Materials and Processing
Keywords: Rheological, Jet printing, Solder paste, Linear visco-elastic, lead-free

Effect of rheological characterization on the jet printing performance of lead-free solder paste

Saipeng Li, Jian Hao, Shuang Tian, Dapeng Wang, Jian Zhou, Feng Xue
Southeast University, China, People's Republic of; lisaipeng@seu.edu.cn

A-18: ID 140

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 140 / A-18: 1
Materials and Processing
Keywords: Finite Element Method, Nanoindentation, TSV, Copper Vias, Response Surface Method

Method for Assessing the Delamination Risk in BEoL Stacks around Copper TSV Applying Nanoindentation and Finite Element Simulation

Jan Albrecht[1], Marie Weissbach[1], Juergen Auersperg[1,2], Sven Rzepka[1]
[1]Micro Materials Center at Fraunhofer ENAS, Germany; [2]Berliner Nanotest und Design GmbH, Germany; jan.albrecht@enas.fraunhofer.de

E-06: ID 153

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 153 / E-06: 1
Materials and Processing
Keywords: passivation polymer, reliability, stress, interposer, redistribution layer

PHOTO-DIELECTRIC POLYMER MATERIAL CHARACTERISATION TO IMPROVE RELIABILITY 3D-IC PACKAGING

Nacima ALLOUTI, Pascal CHAUSSE, Stephane MOREAU, Anais D'AFFROUX
CEA, France; nacima.allouti@cea.fr

E-01: ID 159

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 159 / E-01: 1
Materials and Processing
Keywords: Materials and Processing

Moisture Sensitivity Level One (1) Packaging Solution for a Nickel-Palladium-Gold (NiPdAu) Pre-plated Frames

Alvin Denoyo, Ariel Tan, Jun Berte, Robert Altar
ON Semiconductors, Philippines; Alvin.Denoyo@onsemi.com

B-19: ID 166

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 166 / B-19: 1
Materials and Processing
Keywords: Pb-free solder, high reliability, low temperature soldering, solder hierarchy

High Reliability Low Temperature Pb-Free Alloy for Solder Hierarchy

Pritha Choudhury, Morgana Ribas, Siuli Sarkar
Alpha Assembly Solutions, MacDermid Performance Solutions R&D Centre, India; morgana.ribas@alphaassembly.com

B-04: ID 175

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 175 / B-04: 1
Materials and Processing
Keywords: NCP, Silica Filler, 3D TSV Stack, Warpage, Reliability

The Effects of Silica Filler Content in NCP on the Reliability of 3D TSV Multi-Stack

Wagno Alves Braganca Junior[1], Yong-Sung Eom[2], Jihye Son[2], Keon-Soo Jang[2], Hyun-Cheol Bae[2], Seok Hwan Moon[2], Kwang-Seong Choi[1,2]
[1]University of Science and Technology, Korea; [2]ICT Materials and Components Laboratory, ETRI, Korea; wagnojunior@etri.re.kr

D-13: ID 181

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 181 / D-13: 1
Materials and Processing
Keywords: Low-melting temperature, Solder alloys, Mechanical properties, Flexible and wearable electronics, Indium-Bismuth

Effect of indium on the deformation properties of binary In-Bi alloys

Sanghun Jin[1,2], Min-Su Kim[1], Shutetsu Kanayama[3], Hiroshi Nishikawa[1]
[1]Joining and Welding Research Institute, Osaka University, Japan; [2]Graduate School of Engineering, Osaka University, Japan; [3]Connected Solutions Company, Panasonic Corporation, Japan; passionista82@gmail.com

D-18: ID 189

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 189 / D-18: 1
Materials and Processing
Keywords: Cu /Ni/Sn-Ag microbump, intermetallic compound, electromigration, polarity effect

Electromigration Polarity Effect of Cu/Ni/Sn-Ag Microbumps for Three-Dimensional Integrated Circuits

Hyondong Ryu, Kirak Son, Gahee Kim, Jina Lee, Young-Bae Park
School of Materials Science and Engineering, Andong National University, Korea, Republic of (South Korea); gyehd1231@gmail.com

A-13: ID 191

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 191 / A-13: 1
Materials and Processing
Keywords: Polyimide, Low Dk, Low Df, Transmission loss, Liquid crystal polymer

Low transmission loss flexible substrates using low Dk/Df polyimide adhesives

Takashi Tasaki, Atsushi Shiotani, Takashi Yamaguchi, Keisuke Sugimoto
ARAKAWA CHEMICAL INDUSTRIES, LTD., Japan; tasaki@arakawachem.co.jp

A-08: ID 207

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 207 / A-08: 1
Materials and Processing
Keywords: Heterogeneous Integration, 3D, Packaging, Microfluidics, Stacking, Interconnects

Die Level 3D Heterogeneous Integration of a Microfluidic System

Pavani Vamsi Krishna Nittala, Prosenjit Sen
CeNSE, IISc Bangalore, India; vamsinittala@gmail.com

D-03: ID 230

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 230 / D-03: 1
Materials and Processing
Keywords: High Temperature Materials

High Temperature Endurable Die Attach Material for Power Electronics Package – Process Challenges

Leong Ching Wai, Mian Zhi Ding, GongYue Tang
Institute of Microelectronic, Singapore; wailc@ime.a-star.edu.sg

B-14: ID 231

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 231 / B-14: 1
Materials and Processing
Keywords: Preplated leadframe, plating layer deformation, solderability, scratch test, critical load force

Study of Critical Load Force towards Thin Plating on PrePlated Leadframe

Hui Teng Wang, Chen Ho Ong, Wu Hu Li, Xiao Jun Wang, Lay Peng Ng
Infineon Technologies Asia Pacific, Singapore; huiteng.wang@infineon.com

E-16: ID 254

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 254 / E-16: 1
Materials and Processing
Keywords: Mold Void, Mold Flow, Key mold parameter

Perfect Molding Challenges and The Limitations

Lay Tatt Tan, Yin Yin Teo, Chee Hong Lee, Boon Huat Lim
Infineon Technology (Malaysia), Malaysia; laytatt.tan@infineon.com

D-08: ID 292

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 292 / D-08: 1
Materials and Processing
Keywords: High Elomgation, Package, HAST resistance, Crack resistance, Hgh resolution, Solder Resist, Ball Grid Array

Development of next generation Solder Resist

Nobuhito Komuro, Yuta Daijima, Shinya Imabayashi
Hitachi Chemical, Japan; nobu-komuro@hitachi-chem.co.jp

B-09: ID 296

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 296 / B-09: 1
Materials and Processing
Keywords: RDL dielectric, FOWLP, FOPLP, Photodefinable polyimide, Low-temparature curable

Higher Reliability for Low-temperature Curable Positive-Tone Photosensitive Dielectric Materials

Takenori Fujiwara, Yu Shoji, Yuki Masuda, Keika Hashimoto, Yutaro Koyama, Kimio Isobe, Hitoshi Araki, Ryoji Okuda, Masao Tomikawa
Toray Industries, Inc, Japan; Takenori_Fujiwara@nts.toray.co.jp

Equipment and Process Automation

B-03: ID 172

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 172 / B-03: 1
Equipment and Process Automation
Keywords: Wireless charging, horizontal probe, near field

The Design of Near-Field Horizontal Probe Design for Wireless Charging Coil

Wang Tiang - An, Chen Bo - You, Wu Sung-Mao
National University of Kaohsiung, Taiwan; to0716@gmail.com

B-08: ID 206

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 206 / B-08: 1
Equipment and Process Automation
Keywords: Rc, ICP Sputter Etch, PVD, UBM/RDL, throughput

Indexer PVD Platform – The Key Enabler for High Productivity and Low Contact Resistance for Next-Generation WLP Applications

Patrik Carazzetti, Frantisek Balon, Mike Hoffmann, Juergen Weichart, Andreas Erhart, Ewald Strolz
Evatec AG, Switzerland; patrick.carazzetti@evatecnet.com

B-13: ID 220

Time: Thursday, 07/Dec/2017: 2:00pm - 3:20pm

ID: 220 / B-13: 1
Equipment and Process Automation
Keywords: Scratch test, coating characterization, leadframe coating, tribology, characterization techniques

Scratch Test Methodology for Leadframe Coating

Chen Ho Ong, Alfred Yeo, Hui Teng Wang
Infineon Technologies Asia Pacific, Singapore; chenho.ong@infineon.com

Electrical Simulations & Characterization

C-05: ID 126

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 126 / C-05: 1
Electrical Simulations & Characterization
Keywords: Annular ring routing, plated-through-hole, impedance matching, multi-reflection noise, signal integrity, high-speed signaling

A Novel Annular Ring Design for Improved Plated-Through-Hole Impedance Matching

Jackson Kong[1], Bok Eng Cheah[1], Khang Choong Yong[1], Howard Heck[2]
[1]Intel Microelectronics (M) Sdn. Bhd.; [2]Intel Corporation; jackson.kong@intel.com

C-10: ID 130

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 130 / C-10: 1
Electrical Simulations & Characterization
Keywords: 2.5D silcion optical interposer, 400G, electronic-photonic integrated circuit, RF, high-speed, data center, QSFP, OSFP

2.5D Silicon Optical Interposer for 400G Electronic-Photonic Integrated Circuit Platform Packaging

Do-Won Kim, K. Y. Au, H. Y. Li, X. S. Luo, Y. L. Ye, Surya Bhattacharya, Gou-Qiang Lo

Institute of Microelectronics, Singapore; kimd@ime.a-star.edu.sg

C-15: ID 146

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 146 / C-15: 1
Electrical Simulations & Characterization
Keywords: decoupling, composite capacitor, SRO, three terminals, multiple loads and voltage domains

Efficient Decoupling and Filtering for Multiple Loads and Voltage Domains with Composite Capacitors

Chin Lee Kuan[1], Amit K. Jain[2], Sameer Shekhar[2]
[1]Intel Microelectronics (M) Sdn. Bhd, Malaysia; [2]Intel Corporation, Hillsboro, OR 97124, USA; chin.lee.kuan@intel.com

C-20: ID 180

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 180 / C-20: 1
Electrical Simulations & Characterization
Keywords: FIVR, power integrity, power plane modeling, DC analysis

Distributed DC Electrical Assessment of Switch-Mode Convertors

Sameer Shekhar[1], Amit Kumar Jain[1], Chin Lee Kuan[2]
[1]Intel, United States of America; [2]Intel, Malaysia; sameer.shekhar@intel.com

E-04: ID 186

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 186 / E-04: 1
Electrical Simulations & Characterization
Keywords: electrostatic discharge, near-field

Establish Electrostatic Discharge Simulation Environment Combined with Near-Field measurement

Chia-Hsuan Tsai, Cheng-Dao Li, Sung-Mao Wu
Micro Electrical Packaging Laboratory, Taiwan; st910414@gmail.com

E-09: ID 196

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 196 / E-09: 1
Electrical Simulations & Characterization
Keywords: Dielectric Constant, Near-Field System, transmission line

Dielectric Constant Measurement using Near-Field System

Li-Xuan Tsai, Kuan-I Cheng, Sung-Mao Wu
Micro Electronic Packaging Laboratory, Taiwan; soply0825@gmail.com

E-14: ID 211

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 211 / E-14: 1
Electrical Simulations & Characterization
Keywords: SOLT calibration, SMA to CPWG interface trace characterization, THRU calibration kit.

SMA Connector to Co-Planer Calibration

Chun-Ting Lai
Micro Electronic Packaging Laboratory, Taiwan; locker010313@gmail.com

E-19: ID 228

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 228 / E-19: 1
Electrical Simulations & Characterization
Keywords: Field Programmable Gate Array, System-On-Chip, Automated Test Equipment, Test Floor Automation, Smart Operation

Automation of ATE Test Program Execution in Offline and Online

Deva Ruban Maria, Kamalakannan Viswanathan, Michael Baclay Amal, Karthik Krishna Kumar
Xilinx Asia Pacific Pte. Ltd., Singapore; kvi@xilinx.com

G-05: ID 233

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 233 / G-05: 1
Electrical Simulations & Characterization
Keywords: Low loss transmission line design analysis

Analysis and design of low loss transmission line structure for high speed applications

Mihai Dragos Rotaru
University of Southampton, Malaysia; mdr1f06@soton.ac.uk

G-10: ID 245

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 245 / G-10: 1
Electrical Simulations & Characterization
Keywords: HBM, FOWLP, Electrical simulation, Wide I/Os

FOWLP Design for HBM Applications

Teck Guan LIM
A*STAR IME, Singapore; limtg@ime.a-star.edu.sg

G-15: ID 270

Time: Friday, 08/Dec/2017: 1:50pm - 3:10pm

ID: 270 / G-15: 1
Electrical Simulations & Characterization
Keywords: Surface roughness, TSVs, 3D ICs, Ansys HFSS, Signal integrity

Investigating the Role of Sidewall Surface Roughness on the Performance of Through Silicon Vias

Rohit Y Sharma, Somesh Kumar, Sunil Pathania
Indian Institute of Technology Ropar, India; Somesh.Kumar@iitrpr.ac.in

Mechanical Modeling & Simulations

A-04: ID 119

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 119 / A-04: 1
Mechanical Modeling & Simulations
Keywords: Mechanical simulation, Larger Package, Thin core, Higher electrical performance

Larger FCBGA Package with Thin and Normal Core Evaluation and Characterization

Vito Lin, Nicholas Kao, Don Son Jiang
SPIL, Taiwan; chichshenglin@spil.com.tw

A-09: ID 125

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 125 / A-09: 1
Mechanical Modeling & Simulations
Keywords: ETS MUF FCCSP, temperature-dependent property, temperature-dependent warpage, non-incremental solution based on stress conservation law, trend plot of warpage optimization in 2-dimentional diagram by axes of CTEeff and E.

Trend Plots for Compound Selection Utilized for Warpage Design of MUF FCCSP with 4L ETS

Chih-Sung Chen, Nicholas Kao, Don Son Jiang
Siliconware Precision Industries Co. Ltd. (SPIL), Taiwan; chihsungchen@spil.com.tw

A-14: ID 137

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 137 / A-14: 1
Mechanical Modeling & Simulations
Keywords: FOWLP Power Converter Thermo-mechanical Simulation

Thermo-mechanical Design of Fan-out Wafer Level Package for Power Converter Module

Zhaohui Chen
IME A-Star, Singapore; chenz@ime.a-star.edu.sg

A-19: ID 167

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 167 / A-19: 1
Mechanical Modeling & Simulations
Keywords: ADAS, fatigue life of BGA, variation factor, experimental design method, crack progress analysis

The life cycle impact assessment that the variabilities of BGA solder connection makes

Ryosuke Yano, Qiang YU
Yokohama National University, Japan; yano-ryosuke-tg@ynu.jp

A-24: ID 188

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 188 / A-24: 1
Mechanical Modeling & Simulations
Keywords: near-field coil coupling loss S-Parameter Non-contact measurment

Non-contact Technology by Near-field Measurement

Ping Chia Su, Cheng-Dao Li, Sung-Mao Wu
National University of Kaohsiung, Taiwan, Taiwan; s7616989@gmail.com

C-01: ID 193

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 193 / C-01: 1
Mechanical Modeling & Simulations
Keywords: Strip warpage, finite element, module, dual side molding

Strip Warpage Assessment of Dual Side Molding SiP Module

Ming-Han Wang, Ian Hu, Richard YC Chen, Chan-Lin Yeh, Meng-Kai Shih, David Tarng
Advanced Semiconductor Engineering, Inc, Taiwan; Carter_wnag@aseglobal.com

C-06: ID 194

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 194 / C-06: 1
Mechanical Modeling & Simulations
Keywords: Block Warpage, finite element modeling, dual beam

A Comprehensive Study on BGA Block Warpage and Prediction methodology

Jing-en Luan
STMicroelectronics Pte Ltd, Singapore; jing-en.luan@st.com

C-11: ID 201

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 201 / C-11: 1
Mechanical Modeling & Simulations
Keywords: Vertical die displacement, modulus, bond line thickness, non-stick on pad, bond force

Glue Selection for Robust Wire Bonding Process Related to Non-Stick on Pad

Ee Lin Chung[1], Dandong Ge[2], Chee Mun Wai[1]
[1]Infineon Technologies (Malaysia) Sdn Bhd.; [2]Infineon Technologies Asia Pacific Pte Ltd, Singapore;
EeLin.Chung@infineon.com

C-16: ID 216

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 216 / C-16: 1
Mechanical Modeling & Simulations
Keywords: Shape memory alloy, MEMS, constitutive model, arbitrary loading

Constitutive Model for SMA Considering Arbitrary Thermal-Mechanical Loading and Loading History

Xiaoyong Zhang, Dawei Huang, Mingjing Qi, Xiaojun Yan
Beihang University, China, People's Republic of; zhangxy@buaa.edu.cn

E-05: ID 236

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 236 / E-05: 1
Mechanical Modeling & Simulations
Keywords: wafer warpage, stress, TSV wafer, fine pitch TSV, high density

Study on warpage and stress of TSV wafer with ultra-fine pitch vias for high density chip stacking

Faxing Che, Ling Xie, Zhaohui Chen, Sunil Wickramanayaka
IME, A-star, Singapore,; chenz@ime.a-star.edu.sg

E-10: ID 252

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 252 / E-10: 1
Mechanical Modeling & Simulations
Keywords: Viscoelastic modeling, epoxy mold compound encapsulations, residual stresses, curing behavior

Modeling of manufacturing induced residual stresses of viscoelastic epoxy mold compound encapsulations

Mario Gschwandl[1], Peter Filipp Fuchs[1], Thomas Antretter[2], Mahesh Yalagach[1], Ivaylo Mitev[1], Tao Qi[4], Angelika Schingale[3]
[1]Polymer Competence Center Leoben GmbH, Austria; [2]Intitute of Mechanics, University of Leoben, Austria; [3]Continental Corporation; [4]AT&S; mario.gschwandl@pccl.at

E-15: ID 278

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 278 / E-15: 1
Mechanical Modeling & Simulations
Keywords: 3D IC, Copper Pillar, Reliability

Thermo-Mechanical Reliability Prediction for Copper Pillar 3D IC Devices

Ganesh Hariharan, Raghunandan Chaware, Inderjit Singh, Anandan Ramasamy
Xilinx, United States of America; inderji@xilinx.com

E-20: ID 295

Time: Friday, 08/Dec/2017: 11:00am - 12:20pm

ID: 295 / E-20: 1
Mechanical Modeling & Simulations
Keywords: Board Level Solder, Reliability, Epoxy Mold compound mold, PCB, TMCL

Board Level Solder Reliability Simulation for Epoxy Mold Compound Based Power Package

Qiuxiao Qian[1], Yong Liu[2]
[1]On Semiconductor, China, People's Republic of; [2]On Semiconductor, USA; richard.qian@onsemi.com

Thermal Characterization & Cooling Solutions

C-03: ID 112

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 112 / C-03: 1
Thermal Characterization & Cooling Solutions
Keywords: Heat Exchanger; Data Center; Cooling Solution; Energy Efficiency

Compact Heat Exchanger Design and Energy Efficiency Optimization for Data Centre Cooling Application

GONG YUE TANG, YONG HAN, XIAO WU ZHANG
Institute of Microelectronics, Singapore; tangg@ime.a-star.edu.sg

C-08: ID 134

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 134 / C-08: 1
Thermal Characterization & Cooling Solutions
Keywords: thermal management, hexagonal fins, enhanced microchannel, electronics cooling, heat sinks

Experimental Investigation of Microchannel Heat Sink with Modified Hexagonal Fins for Electronics Cooling

Sellakkutti Subramanian[1], K.S Sridhar[2], C.K Umesh[3]
[1]Microwavetube Research and Development Centre, Bangalore, India; [2]PES Institute of Technology,Bangalore, India; [3]University Visvesvaraya College of Engineering,Bangalore University,Bangalore, India; subramanian3669@gmail.com

C-13: ID 135

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 135 / C-13: 1
Thermal Characterization & Cooling Solutions
Keywords: liquid cooling, data center, micro-fluid heat snk, jet impingement, high performance processor

Hybrid Micro-Fluid Heat Sink for High Power Dissipation of Liquid-Cooled Data Centre

Yong Han, Gongyue Tang, Boon Long Lau, Xiaowu Zhang
Institute of Microelectronics, A*STAR, Singapore; hany@ime.a-star.edu.sg

C-18: ID 155

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 155 / C-18: 1
Thermal Characterization & Cooling Solutions
Keywords: Si interposer; heat sink; inlet and outlet

Optimal Design of a microchannel heat sink with a pin-fin array integrated with Si interposer

Yunna Sun, Taegyu Kang, Jian Li, Zhiyu Jin, Xinyue Chang, Yan Wang, Zhuoqing Yang, Guifu Ding
Shanghai Jiao Tong University, China, People's Republic of; Cecilia_Sun@sjtu.edu.cn

D-04: ID 171

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 171 / D-04: 1
Thermal Characterization & Cooling Solutions
Keywords: SIP(System in package), double side modeling, thermal simulation, thermal measurement

Thermal Characterization of Dual Side Molding SiP Module

Tang-Yuan Chen, Bo-Syun Chen, Jin Feng Yang
Advanced Semiconductor Engineering Inc., Taiwan; Phidia_Chen@aseglobal.com

D-09: ID 173

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 173 / D-09: 1
Thermal Characterization & Cooling Solutions
Keywords: LED characterization, LED measurement, multiphysics modelling

Measurement issues in LED characterization for Delphi4LED style combined electrical-optical-thermal LED modeling

Marta Rencz[1,2], Gusztav Hantos[2], Janos Hegedus[2], Marton Bein[1], Lajos Gaal[1], Gabor Farkas[1], Zoltan Sarkany[1], Sandor Ress[1,2], Andras Poppe[1,2]
[1]Mentor Graphics, Hungary; [2]Budapest University of Technology; Marta_rencz@mentor.com

D-14: ID 192

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 192 / D-14: 1

Thermal Characterization & Cooling Solutions

Keywords: termal simulation, Dual-Phase-Lag, Fourier-Kirchhoff, FinFET, GAAFET

Comparison of temperature distribution in FinFETs and GAAFETs based on Dual-Phase-Lag heat transfer model

Tomasz Raszkowski, Agnieszka Samson, Mariusz Zubert, Marcin Janicki

Lodz University of Technology, Poland; traszk@dmcs.pl

D-19: ID 265

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 265 / D-19: 1

Thermal Characterization & Cooling Solutions

Keywords: Switched Reluctance motor, Thermo-hydrodynamic Analytical, cooling system, boiling, liquid immersion

Development of the high efficiency cooling structure of the liquid immersion cooling SR motor

Daiki Wakabayashi[1], Qiang YU[1], Yoshinobu Nakamura[2]

[1]Yokohama National University, Japan; [2]NIDEC CORPORATION, Japan; wakabayashi-daiki-pk@ynu.jp

Quality, Reliability & Failure Analysis

A-05: ID 109

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 109 / A-05: 1

Quality, Reliability & Failure Analysis

Keywords: NiPdAu, discoloration, surface, diffusion

Can subsurface diffusion manifest as discoloration in NiPdAu surface?

Ian Harvey Arellano, Lady Marianne Polinga, Ernesto Jr Antilano

STMicroelectronics, Inc., Philippines; ian-harvey.arellano@st.com

A-10: ID 113

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 113 / A-10: 1

Quality, Reliability & Failure Analysis

Keywords: Accelerated testing, Power cycling, FEM, Coffin-Manson, Fatigue

Reliability Prediction of LED Packaging by Fatigue Behavior of Bonding Wire in Power Cycling Accelerated Test

Yongjun Pan[1], Fulong Zhu[1], Xinxin Lin[1], Fengren Wang[1], Lang Shi[1], Yan Kan[1], Sheng Liu[1,2]

[1]School of Mechanical Science and Engineering, Huazhong University of Science and Technology, China; [2]School of Power and Mechanical Engineering, Wuhan University, China; yongjun_pan@hust.edu.cn

A-15: ID 123

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 123 / A-15: 1

Quality, Reliability & Failure Analysis

Keywords: Reliability, wearable electronics, water proof test, smartwatch, electronic product design

Reliability of wearable electronics - case of water proof tests on smartwatch of Xiaomi Mi Band 2

Yuk Ngang Zita Yip

City University of Hong Kong, Hong Kong S.A.R. (China); zitayip.yyn@my.cityu.edu.hk

A-20: ID 142

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 142 / A-20: 1
Quality, Reliability & Failure Analysis
Keywords: Leakage Current Failures, QFN-mr, Waterjet Deflash

Resolution of Leakage Current Failures on QFN-mr Devices by Optimizing Waterjet Deflash Process

Frederick Ray Insular Gomez, Tito Jr Tubana Mangaoang, Daniel Jr Lalangan Burguillos
Back-End Manufacturing & Technology, STMicroelectronics, Inc., Philippines; frederick-ray.gomez@st.com

A-25: ID 154

Time: Thursday, 07/Dec/2017: 10:30am - 12:10pm

ID: 154 / A-25: 1
Quality, Reliability & Failure Analysis
Keywords: Solder interconnect; Electromigration (EM); microstructure; test vehicles; limitations

Review on test vehicles for electromigration (EM) study in solder interconnects

Ze Zhu[1], Yan-cheong Chan[1], Fengshun Wu[2], Chee Lip Gan[3], Zhong Chen[3]
[1]City University of Hong Kong, Hong Kong S.A.R. (China); [2]Huazhong University of Science and Technology, China; [3]Nanyang Technological University, China; eeycchan@cityu.edu.hk

C-02: ID 163

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 163 / C-02: 1
Quality, Reliability & Failure Analysis
Keywords: Risk assessment, HHM, DRBFM, MF-RA

Risk Assessment Study of New Product Development

Kazuaki Ano
Dialog Semiconductor, Japan; kazuaki.ano@diasemi.com

C-07: ID 164

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 164 / C-07: 1
Quality, Reliability & Failure Analysis
Keywords: Failure Analysis, Reliability, Copper pillar, Electromigration, Package

Application of Failure Analysis on Package Copper Pillar Bump Electromigration

Wei-Chiao Wang, Kuan-I Cheng, Sung-Mao Wu
Micro Electrical Packaging Laboratory, Taiwan; josephgun125@gmail.com

C-12: ID 165

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 165 / C-12: 1
Quality, Reliability & Failure Analysis
Keywords: Vapour phase, reliability, defluxing, lead free, toxicity

Optimization Of Chemistry For A Vapour Phase Process To Deflux No Clean Lead Free Materials On PCBs

Patrick J. Duchi, Jonathan Cetier, Laurent Levasseur, Jacquemine Coquio, Rodrigo Aguilar
Inventec Performance Chemicals; ccheu@inventec.dehon.com

C-17: ID 197

Time: Thursday, 07/Dec/2017: 4:40pm - 6:00pm

ID: 197 / C-17: 1
Quality, Reliability & Failure Analysis
Keywords: Resolution degration, Scanning acoustic microscopy, defect

Scanning Acoustic Microscopy: Resolution Reduction due to Attenuation of Acoustic Signal in Materials

Chiu Soon Wong
Infineon Technologies (Malaysia) Sdn. Bhd., Malaysia; chiusoon.wong@infineon.com

D-05: ID 198

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 198 / D-05: 1
Quality, Reliability & Failure Analysis
Keywords: Power cycling

The influence of the cycling parameters on the reliability test results of IGBTs

Zoltan Sarkany[1], Marta Rencz[1,2]
[1]Mentor Graphics, Hungary; [2]Budapest University of Technology and Economics; zoltan_sarkany@mentor.com

D-10: ID 243

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 243 / D-10: 1
Quality, Reliability & Failure Analysis
Keywords: quality assurance, non-destructive testing methods, measurement characteristic, process characteristic

Measuring methods and measuring errors in electronics production technologies

Martin Oppermann, Thomas Zerna
Technische Universitaet Dresden, Centre for Microtechnical Manufacturing; martin.oppermann@tu-dresden.de

D-15: ID 268

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 268 / D-15: 1
Quality, Reliability & Failure Analysis
Keywords: Junction stain, scanning capacitance microscopy, compound semiconductor, Gallium Arsenide, selective etching

GaAs Device Two-Steps Junction Stain and Scanning Capacitance Microscopy Sample Preparation

Yih-Sheng Chuang, Chun-An Huang, Ju-Hung Hsu, Yung-Jen Wu
Integrated Service Technology; frank_chuang@isti.com.cn

D-20: ID 279

Time: Friday, 08/Dec/2017: 9:00am - 10:20am

ID: 279 / D-20: 1
Quality, Reliability & Failure Analysis
Keywords: fatigue, thermal, mechanical, combined loads

Solder Joint Fatigue Analysis under Combined Thermal and Vibration Loading

Karsten Meier[1], Mike Roellig[2], Yifan Liu[1], Karlheinz Bock[1]
[1]Technische Universität Dresden, Electronics Packaging Laboratory, Germany; [2]Fraunhofer Institute for Ceramic Technologies and Systems - Material Diagnostics, Germany; karsten.meier@tu-dresden.de

INTERACTIVE Presentations

Interactive session #1

Time: Thursday, 07/Dec/2017: 10:00am - 10:30am

ID: 301 / Coffee/Tea Breaks #1: 1
Interconnection Technologies
Keywords: Power electronics, additive manufacturing, interconnection technology, copper wire bonding

Investigations of Copper Wire Bonding Capability on Plasma Based Additive Copper Metallizations

Alexander Hensel[1], Klaus Kohlmann von Platen[2], Joerg Franke[1]
[1]Institute for Factory Automation and Production Systems (FAPS), Friedrich-Alexander-University Erlangen-Nuremberg; [2]Fraunhofer Institute for Silicon Technology (ISIT); alexander.hensel@faps.fau.de

ID: 259 / Coffee/Tea Breaks #1: 2
Thermal Characterization & Cooling Solutions
Keywords: Electro-thermal measurement, die attach, transient thermal performance, wafer prober

Evaluation of Die Attach Process Quality using Transient Electro-thermal Measurement Technique

Kai Yang[1], Alfred Yeo[1], Yuen Sing Chan[1], Xiaojun Terry Wang[1], Dirk Schweitzer[2]
[1]Infineon Technologies Asia Pacific Pte Ltd; [2]Infineon Technologies AG; Kai.Yang@infineon.com

ID: 285 / Coffee/Tea Breaks #1: 3
Emerging Technologies
Keywords: smart packaging, internet of things, flexible hybrid electronics

Hybrid flexible smart temperature tag with NFC technology for smart packaging

Xi Zhang, Xuechuan Shan
Singapore Institute of Manufacturing Technology, Singapore; zhangxi@Simtech.a-star.edu.sg

ID: 241 / Coffee/Tea Breaks #1: 4
Materials and Processing
Keywords: Molding, FOWLP, mold voids

Process Development of Moldable Underfill on Fine Pitch RDL 1st Fan-out Wafer Level Package

Simon Siak Boon Lim, Mian Zhi Ding, Ser Choong Chong
Institute of Microelectronics, Singapore; limsb@ime.a-star.edu.sg

ID: 251 / Coffee/Tea Breaks #1: 5
Interconnection Technologies
Keywords: Cu nanoparticle, Electronics, Reflow bond, Resistance, Mechanical test

Copper nanoparticle paste on different metallic substrates for low temperature bonded interconnection

Jaewon Kim[1], Byunghoon Lee[2], Ja-Myeong Koo[2], Chee Lip Gan[1]
[1]Nanyang Technological University, Singapore; [2]Global technology center, Samsung Electronics, Yeongtong-Gu, Suwon-si, Korea; jwkim@ntu.edu.sg

ID: 138 / Coffee/Tea Breaks #1: 6
TSV/Wafer Level Packaging
Keywords: flip chip, wafer level packaging

Chip-to-Wafer (C2W) flip chip bonding for 2.5D High density interconnection on TSV free interposer

Pei Siang Lim, Mian Zhi Ding, Masaya Kawano
Institute of Microelectronics, Singapore; limps@ime.a-star.edu.sg

ID: 276 / Coffee/Tea Breaks #1: 7
Emerging Technologies
Keywords: Stretchable circuits, screen printing, carbon nanostructures, silver nanostructures

Mechanical And Electrical Characteristics Of Screen Printed Stretchable Circuits On Thermoplastic Polyurethane

Sihan Joseph Chen[1], Xuechuan Shan[1], Reuben Tang[2], Vasudiva Sunappan[1], Zhaowei Zhong[2], Jun Wei[1]

[1]Singapore Institute of Manufacturing Technology; [2]MAE, Nanyang Technological University; shchen@SIMTech.a-star.edu.sg

ID: 150 / **Coffee/Tea Breaks #1: 8**
Emerging Technologies
Keywords: battery-less LED, endoscopic clip, LC circuit, Cockcroft-Walton Circuit, laparoscopic surgery

Development of the Endoscopic Clip with a Battery-Less LED for Laparoscopic Gastrointestinal Resection

Kyohei Shibata[1], Yuharu Shinki[1], Ryosuke Tsutsumi[2], Tetsuo Ikeda[2], Haruichi Kanaya[1]
[1]Kyushu University, Japan; [2]Kyushu University Hospital, Japan; 2ie16656p@s.kyushu-u.ac.jp

ID: 225 / **Coffee/Tea Breaks #1: 9**
Emerging Technologies
Keywords: Thin Fim Encapsulation, MEMS, Wafer level packagaing

Evaluation of Thin Film Encapsulation strength for commercial packaging

Jae-Wung Lee, Srinivas Merugu, Ser Choong Chong, Navab Singh
Institute of Microelectronics, Singapore; leejw@ime.a-star.edu.sg

ID: 182 / **Coffee/Tea Breaks #1: 10**
Electrical Simulations & Characterization
Keywords: FOPoP, SI, PI

Design and Electrical Analysis for Advanced Fan-out Package-on-Package

Pan Po-Chih, Hsieh Tsun-Lung, Huang Chih-Yi, Jhong Ming-Fong, Wang Chen-Chao
Advanced Semiconductor Engineering Group, Taiwan; Powei_Pan@aseglobal.com

ID: 234 / **Coffee/Tea Breaks #1: 11**
Emerging Technologies
Keywords: back-end process for implants; iridium oxide; Parylene C

Development of Back-end Process Integration for Implantable Neurostimulation Application

PO-CHUN CHEN, Heng-An Ku, Pin-Cheng Lin
National Taipei University of Technology, Taiwan; cpc@mail.ntut.edu.tw

ID: 262 / **Coffee/Tea Breaks #1: 12**
Materials and Processing
Keywords: Ag sintering, die attach, low-temperature sintering, pressure-less

Metallic Bond Development On Power Package- Ag Sintering Material

ChienHao Wang, Bob Lee
Texas Instruments, Taiwan; howardwang@ti.com

ID: 226 / **Coffee/Tea Breaks #1: 13**
Thermal Characterization & Cooling Solutions
Keywords: TSI cooling solution

Thermal Design and Analysis of Through Silicon Interposer (TSI) Package

LIN BU
IME, Singapore; bul@ime.a-star.edu.sg

ID: 284 / **Coffee/Tea Breaks #1: 14**
Materials and Processing
Keywords: sintered silver nanoparticles, nanomechanical property, elastic modulus, hardness, creep stress exponent

Nanomechanical Properties of Pressure-Less Sintered Silver Nanoparticles

Xu Long[1], Wenbin Tang[1], Weijuan Xia[2]
[1]Northwestern Polytechnical University, China, People's Republic of; [2]Space Research Institute of Electronics and Information Technology, Aerospace Science and Technology Corporation; xulong@nwpu.edu.cn

ID: 242 / **Coffee/Tea Breaks #1: 15**
Materials and Processing
Keywords: Thin wafer handling, Advanced packaging, Room temp. debonding, Single layer adheisve, TBDB

Evaluation of Single Layer Adhesive Material for Thin Wafer Handling Applications

Nagendra Sekhar Vasarla[1], Hongmiao JI[1], Shinji ARIMOTO[2], Toru OKAZAWA[2], Takenori FUJIWARA[2], Masaya KAWANO[1]
[1]Institute of Microelectronics, Singapore; [2]Toray Industries, Inc., Japan; vasarla@ime.a-star.edu.sg

ID: 215 / **Coffee/Tea Breaks #1: 16**
TSV/Wafer Level Packaging
Keywords: coaxial-annular through silicon via (CA-TSV), three-dimensional (3-D) integrated circuit (IC), wideband modeling

Wideband Modeling and Characterization of Coaxial-annular through-silicon via for 3-D ICs

Zheng Mei, **Gang Dong**
Xidian University, China, People's Republic of; mmzzkkxx@126.com

Interactive session #2

Time: Friday, 08/Dec/2017: 3:10pm - 3:40pm

ID: 149 / **Coffee/Tea Break #04: 1**
Materials and Processing
Keywords: Chemical Deflash, Adhesive Residue, QFN, Plasma

Addressing the persistent adhesive residue problem in taped QFNs

Ernesto Tarosan Antilano Jr, Ian Harvey Arellano
STMicroelectronics, Philippines; ernesto.antilanojr@st.com

ID: 238 / **Coffee/Tea Break #04: 2**
Materials and Processing
Keywords: underfill, 3DIC, large die, pattern, SAT

Study of underfill dispensing for a large-die package

Huei Nuan Huang, Matt Tseng, Chung Liang Liu, Cheng Sheng Xu, Kun Hung Lin, Che Min Chu, Yu Huci Tsai
SPIL, Taiwan; hnhuang@spil.com.tw

ID: 229 / **Coffee/Tea Break #04: 3**
TSV/Wafer Level Packaging
Keywords: Wafer level packaging, mold compound, RDL, material characterization, millimeter wave

Characterization of Molding Compound Material and Dielectric of RDL Layers

Zihao Chen, Teck Guan Lim
IME, A*STAR, Singapore; chenzh@ime.a-star.edu.sg

ID: 219 / **Coffee/Tea Break #04: 4**
Quality, Reliability & Failure Analysis
Keywords: wirebond, copper, bond pad, reliability, high temperature storage

Factors affecting activation energy for Pd-coated Cu ball bond resistance degradation on Al bond pads in high temperature storage

Stevan G Hunter[1], Michael D Hook[2], Michael Mayer[2]
[1]ON Semiconductor, United States of America; [2]University of Waterloo; sputterman0@gmail.com

ID: 302 / **Coffee/Tea Break #04: 5**
Quality, Reliability & Failure Analysis
Keywords: Primer process; lead delamination ; broken wedge; 75um Al wire; DOE

Study on the Impact of Primer Process Control and Lead Delamination Towards Cracked/ Broken Wedge Bond

SHU HUI GOH, **CHEE KIANG LAU, KIM SENG CHANG**
Infineon Technology, Malaysia; SHUHUI.GOH@INFINEON.COM

ID: 133 / **Coffee/Tea Break #04: 6**
Mechanical Modeling & Simulations
Keywords: Cu wire bonding, Cu-Al IMC, interfacial stress, FEA simulation

MODELLING OF WIRE BONDING CU-AL INTERMETALLIC FORMATION GROWTH TOWARDS INTERFACIAL STRESS

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ID: 129 / **Coffee/Tea Break #04: 7**
Mechanical Modeling & Simulations
Keywords: underfill, simulation, FCBGA, bump, dispersion

Package with Simulation Method To Predict Underfill Flow Pattern with Different Dispensed Condition

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ID: 255 / **Coffee/Tea Break #04: 8**
Advanced Packaging
Keywords: Glass interposer, transmission line, RF loss

The fabrication of transmission line on the glass substrate

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ID: 257 / **Coffee/Tea Break #04: 9**
Electrical Simulations & Characterization
Keywords: Inductance, Electrical Simulation, Wiresweep Simulation, GQFN

Inductance Characterization and Improvement on a Small GQFN Package

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ID: 289 / **Coffee/Tea Break #04: 10**
Materials and Processing
Keywords: polymer dielectrics, photo voltaic, failure characterization

The mechanism and damage of snail trails

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ID: 156 / **Coffee/Tea Break #04: 11**
Quality, Reliability & Failure Analysis
Keywords: Flux, Solder Paste, EDX, High-side Switch, Ultrasonic

Qualitative & Quantitative Study of Flux-clean Solution for Smart High-Side Device

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ID: 273 / **Coffee/Tea Break #04: 12**
Emerging Technologies
Keywords: Device, Multiferroic, Nanpparticles, Sol-gel, Band gap

Enhancing magnetoelectric and optical properties of co-doped bismuth ferrite multiferroic nanostructures

Matin MD Abdul[1], Hossain M. N.[1], Mozahid F. A.[1], Islam M.R.[1], Rizvi M. H.[1], Hussain A.[1], Rahman M. M.[2], Islam M. F.[1]
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ID: 147 / **Coffee/Tea Break #04: 13**
Equipment and Process Automation
Keywords: Linear motor, High-precious, Synchronous planing control, Decoupling control

Research on Dual-Linear Motor Synchronous Control in the High-precision Gantry Motion Stage

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ID: 271 / **Coffee/Tea Break #04: 14**
Mechanical Modeling & Simulations
Keywords: regression, optimization, layout, packaging, circuit

Using Regression Analysis to Optimize the Layout of Substrate Circuit

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ID: 136 / **Coffee/Tea Break #04: 15**
Quality, Reliability & Failure Analysis
Keywords: Failure Analysis, through silicon via (TSV), Time-domain Reflectometry (TDR), high-resolution, impulse wave simulation

2.5D Chip TSV Open Failure Analysis by High Resolution Time-domain Reflectometry

Masaichi Hashimoto[1], Makoto Shinohara[1], Yang Shang[1], Aparna Mohan[2], Bernice Zee[2]
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ID: 106 / **Coffee/Tea Break #04: 16**
Thermal Characterization & Cooling Solutions
Keywords: Three-Dimensional ICs, Through Silicon Via, Thermal, Challenges.

Survey on 3D-ICs Thermal Modeling, Analysis, and Management Techniques

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ID: 274 / **Coffee/Tea Break #04: 17**
Materials and Processing
Keywords: Image processing, Rough leadframe, C#

High Accuracy Image Processing Technology Developed for Rough Leadframe and Quality Assurance

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ID: 240 / **Coffee/Tea Break #04: 18**
Quality, Reliability & Failure Analysis
Keywords: Supply Chain, Supply Chain Management, Reverse Supply Chain, Analytics, Industrie 4.0, IoT, Big Data, Internet of Things, Predictive, Prescriptive, Cognitive, Descriptive, Data Management, Data Source, Systems of Engagement, Systems of Records, Quality, C

Predictive Analytics in Reverse Supply Chain Management - Commodity Life Expectancy for Quality Engineering

Ai Kiar Ang, Alfred Degbotse, Julian SK Tan, Ngoc Vuong Quy
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