Opening Keynote #1

Extending Moore's Law with Advanced Packages

Abstract: Since the advent of integrated circuit technology in 1958, the integration has been primarily monolithic. Unfortunately, due to physical and economic reasons, the vast majority of analog chips, digital chips, and memory chips are each built on separate technologies. Therefore, in order to deliver optimum system performance, power, and cost, it is desirable to integrate multiple different die, each using its own optimized technology, in a single package. Advanced packaging technologies, e.g. 3DIC, SSIT(stacked silicon Interconnect technology) etc., have been developed to extend scaling beyond the Moore's Law to achieve higher transistor count, increased functionality and superior performance.

Xilinx is the leading provider of all programmable FPGA (Field Programmable Gate Array) products. To achieve high performance, but low power and cost, Xilinx has developed an innovative SSIT technology that employs microbumps and through-silicon vias (TSVs) to integrate multiple FPGA die slices placed side-by-side on a passive silicon interposer, and successfully delivered the industry's first 28nm homogeneous SSIT device. This technology is further developed for advanced technical nodes (20nm, 16nm and beyond) to allow integrating heterogeneous components such as Processor, FPGA, GPU, Memory, Serdes, etc. on the same interposer die enabling faster computing through reduced latency.

The advance of packaging and assembly technology will be introduced, and the benefits of advanced packaging to the various products will be highlighted. Successful qualification of these products is driving the high growth in the applications e.g. cloud computing, embedded vision, industrial IOT, and 5G wireless etc.

Bio: WK Wong serves as Vice President of Corporate Quality, chartered to lead the definition, deployment and establishing of engineering, systems, cultural and customer relationship aspects of delivering Xilinx products to the highest quality standards.

Among WK's global responsibilities are Quality methods, Engineering tools, industry systems and standards, supply chain quality, customer quality engineering, document control, device failure analysis and reliability engineering. He leads a worldwide quality organization chartered with driving continuous improvement of the company's corporate quality methodology for design, manufacture, training, measurement, and post-sale customer support for Xilinx products. Together with the worldwide sales team, WK actively engages customers to position Quality as an essential enabling factor in developing new business opportunities.

WK has 27 years' experience in the Semiconductor industry with Intel Corp, Avago Corp and Xilinx. Prior to his position in Corporate Quality, he served in various positions in Process development, Product and Test engineering, New Product Introduction and Mobile device R&D.

Wong holds a B.Eng. in Electronics and Electrical engineering from the Science University of Malaysia and an MBA from the University of Bath, United Kingdom.

W.K. Wong

Xilinx Vice President

Corporate Quality

Opening Keynote #2

The Evolution of Packaging Technology for Mobile Platforms – Where We have been and where we are headed

Dr. Raj Pendse

Abstract: With the plateauing of Moore's Law for semiconductors, we are at a watershed moment in the evolution of Packaging technology, especially for the demanding use cases presented by the myriad manifestations of Mobile products.

We will look at the progression of Packaging technology for Mobile platforms starting with traditional packaging approaches, to the rapid adoption of Flip Chip and Wafer-level Packaging and the future direction as we enter the realm of 5G, the convergence of Cellular and Computing and last but not the least, the rapid emergence of Automotive electronics. We will map the trends in the various emerging implementations of Mobile technology, such as High band width/ low latency Wireless communication, Virtual/ Augmented Reality and IOT's into the corresponding implications for the underlying Semiconductor and Packaging technologies and highlight the fundamental technology elements that are likely to drive the Packaging direction going forward.

Bio: Dr. Raj Pendse leads Packaging Strategy at Qualcomm, covering core Packaging technology for Application Processors, Modems and RF/Analog devices and use cases in Mobile and adjacent markets like Automotive and Servers.

Prior to Qualcomm, Raj held leadership roles at STATSChipPAC (now JCET), Hewlett-Packard Labs and National Semiconductor, where his work spanned the areas of Packaging for high-end microprocessors, ASIC's, GPU's and low-cost packaging solutions for Consumer hardware. His most recent focus has been on new Packaging for 5G which includes novel approaches like SoC partitioning, new Memory integration schemes and mm wave RF & antenna integration.

Raj completed his BS in Materials Science from IIT Bombay with Top in Class honors and his Doctorate in Materials Science from UC Berkeley.

Raj Pendse

Qualcomm

Closing Keynote Talk

Design tools and modelling for power electronics packages – current status and future challenges

C Bailey

University of Greenwich

Abstract

Packaging of power semiconductors and passives is seeing significant changes. For example, the use of wide band gap devices (SiC and GaN) is set to accelerate, and advanced packaging technologies such as die embedding, chip-on-board, and press-pack assembly are now being developed. New materials such as sintered interconnects are also being for interconnects.

To support development and application of these packaging technologies, modelling and simulation tools need to address a wide range of interacting physical phenomena. This presentation details the current status of modelling tools for power electronics packaging and details the challenges for electrical, thermal, reliability and robustness analysis. For example, the need for multi-domain, multi-scale and multi-objective optimisation toolsets will be discussed. The presentation will provide examples of current modelling toolsets and discuss future challenges.

Bio:

Professor Bailey is Director of the Computational Mechanics and Reliability Group at the University of Greenwich, UK. He has a PhD in Computational Modeling, and an MBA in Technology Management. He joined the University of Greenwich in 1991 after a three-year post-doctoral fellowship at Carnegie-Mellon University. He has published over 300 papers on Design and Simulation of micro/nano-technology based processes and products and has managed many UK and International projects and worked closely with over 100 companies with regards their design, simulation and modelling requirements.

In 2003 he was the Royal Society visiting Professor to Hong Kong. In 2007 he was and Programme Chair for High Density Packaging Conference in Shanghai, China, and also the local organizer of the IEEE sponsored EuroSime conference in London. In 2008 he was the General Chair for the Electronics System-integration Technology Conference (ESTC-2008) in Greenwich, London, and organiser of the Therminic Workshop in 2014. He is a member of the Board of Governors for IEEE EPS, Vice-President for EPS coference, and is UK Chapter Chair for the IEEE EPS and Reliability Societies. Chris is also leading the modelling and simulation activities on the new Heterogeneous Integration Roadmap.

Invited Presentations

Invited presentation 1: Enhanced Bonding Technology for Hybrid Integration in 3D Packaging Technology

Guilian Gao, L.W. Mirkarimi, G. Fountain, S. Arkalgud, Liang Frank Wang and Bongsub Lee

Xperi, 3025 Orchard Parkway, San Jose, CA 95129, USA

Abstract

Continuous miniaturization of electronic devices is driving the growth of 3D packaging in multiple markets segments including mobile, Internet of Things (IOT), and automotive. System in Package (SIP) and Micro-Electro-Mechanical Systems (MEMS) applications are proliferating multiple markets. Enhanced functionality with component size reduction are expected in the next generation products while the average sales price (ASP) is falling. Additionally, the automotive market demands highly accurate, low temperature or vibration drift adding additional pressure for cost-effective solutions. Die shrink is a natural choice for cost reduction for both SIP and MEMs. Streamline manufacturing with one bond technology that serves multiple applications is attractive for driving down cost. The dielectric bonding technology (ZiBond) and hybrid bonding technology (Direct Bonding Interconnect or DBI) are platform technologies, which offer higher yield, lower cost of ownership and the potential of electrical interconnect through the bond line. The DBI technology forms a dielectric-to-dielectric bond at room temperature and ambient pressure and then establishes metal-to-metal connection (usually Cu-to-Cu bond) by a low temperature batch annealing (150 – 300^{o}C).

This talk includes an analysis of the SIP and MEMS market trends and requirements, a brief introduction of the hybrid bonding technology in wafer-to-wafer and die-to-wafer applications. The challenges and advantages of ZiBond and DBI technology compares the conventional bond techniques in MEMs. The bond strength and hermeticity of ZiBond prototype cavity packages are studied. ZiBond and DBI technologies offer a bonding process with superior bond strength of 120—180 MPa, compared to 10-15 MPa reported for anodic bonding. Other MEMs bonding techniques, Eutectic and glass frit, are also evaluated. The electrical performance and assembly yield data for prototypes built with die-to-wafer (D2W) are discussed.

D2W technology for SIPs is attractive as the bonding surface is simply an extension of the dielectric and metal layer of the die back end of line (BEOL), so the conventional thermal compression bonding (TCB) of solder micro bumps is no longer required. Compared to the low throughput of microbump TCB process, DBI offers an elegant solution with short bond dwell times (~0.1 seconds for dielectric bonding) and batch anneal processes, which significantly enhances the overall throughput. The bond interface contains only Cu and dielectric, with no solder or other adhesives. Consequently, the thermal-mechanical stress from the interconnect is reduced, thus enabling further die thickness reduction without compromising performance. Another significant breakthrough is the drastic increase of interconnect density. Interconnect pitch for micro bump TCB is currently around 40µm, or 625 interconnects per mm^2 and further pitch reduction is extremely difficult. However, with the DBI technology, the interconnect pitch scalability follows the lithographic and bonder alignment capability to micron-level pitches. This technology is capable of greater than 1 million interconnects per mm^2 for pitch scaling in X-Y dimension. The combination of ultrahigh interconnect density in the X-Y dimension and ultrathin die in Z direction enables

chip designer to re-configure ICs from 2D design to 3D design to achieve significant power reduction and electrical performance enhancement. Furthermore, the technology is fully compatible with BEOL wafer fabrication processes and can reduce the overall cost of ownership.

Bio: Guilian Gao received her Ph.D. in Materials Science from University of Cambridge, U.K, her M.S. in Corrosion and Protection from University of Manchester, U.K and her B.S. in Materials Science and Engineering from Beihang University, China. Dr. Gao has 27 years of experience in electronics packaging technology development, materials, processes and reliability engineering. She is currently a Principal Engineer in 3D Technology at Xperi Corp. in San Jose, CA. Prior to her Xperi assignment, she was a Staff Engineer and Program Manager at Tessera Inc. Before joining Tessera, she was a Senior Technical Specialist at Ford Motor Co. and was awarded the Henry Ford Technology Award. Dr. Gao holds 29 US patents and more than 30 publications.

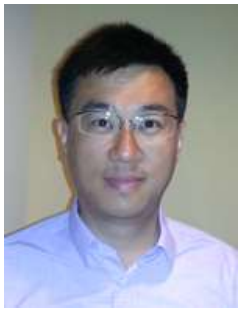
Invited presentation 2: Packaging of Integrated Silicon Photonic devices: Electrical, Optical, Thermal Challenges and Applications

by Jun Su Lee, Senior Packaging Researcher, Photonics Packaging group, Tyndall National Institute

Abstract: As increasing demands for integrated photonic devices in data centers, telecommunications and sensors, various silicon photonic devices are being developed. Accordingly the Si-photonic modules are designed with various packaging prototype structures in development. The optimization of packaging configurations is indispensable for Si-photonic devices to be productized or to be tested out of the research labs. Although the packaging structures and requirements of Si-photonic devices can be diverse by their applications, Si-photonic packaging can be simplified into the three parts of electronics, optics and thermal management, and all of these three factors must to be comprehensively considered for planning the Si-photonic packaging. In this presentation, we are going to discuss the challenges of photonic packaging through the cases of Si-photonic packaging developments at Tyndall National Institute. Technologically as for electronic, optical packaging and thermal management respectively, this presentation contains fine pitch Cu pillar flip-chip bonding, optical fiber alignment on photonic integrated chips, and thermal modeling using a FEM simulation. Lastly, Si-photonics packaging service at Tyndall National Institute and PIXAPP program of open-access photonic integrated circuit (PIC) assembly and packaging pilot line will be briefly introduced.

Bio: Jun Su Lee received his PhD degree in microsystems (in Electronic Engineering) from Imperial College London, UK in 2006. He moved to Korea and worked at Amkor

Technology Korea as a senior researcher to develop electronics packaging from 2006 to 2010. And then he worked as a principal researcher at Samsung Advanced Institute of Technology (SAIT) for leading a project of medical X-ray detector development from 2010 to 2012. After that, he worked at Institute of Microelectronics in Singapore as a scientist II to develop MEMS integration from 2012 to 2013. Currently he is working at the Tyndall National Institute in Ireland as a senior packaging researcher in the Photonics Packaging Group from 2013. He has been leading EU funded research projects and the development projects of industrial companies. His research activities focus on flip-chip bonding and optical packaging for optoelectronic devices in Si-photonics.



Invited presentation 3: Innovative Process and Equipment Technology Solutions for 3D SiP Packaging by Albert Lan

Abstract: The 1st successful 2.5D IC - FPGA has been launched in 2012 for homogeneous partitions and followed up by heterogeneous device integration by GPU & 3D IC HBM since 2015. Moreover, Fan-Out technology were also brought into AP/BB mobile devices and HVM in year2016. All of them are based on advanced 3D SiP building blocks.

IC industry are looking for more cost effective packaging solutions, and innovative technology methodologies, including TSV-less or Fan-Out techniques toward higher integration adoptions, such as VR/AR and AI, for IOT era.

Some innovative process and equipment technology and cost effective solutions for 3D SiP Packaging will be introduced in the talk.

Bio: Mr. Albert Lan / 藍章益 先生, Global Packaging TD, Applied Materials

Education:

- Master of industrial & mechanical engineering department, Univ. of Wisconsin, Madison.

Experience:

- Over 25 years of job experience in semiconductor industry, especially focusing on advanced packaging technologies.
- Senior R&D Director, 13 years, SPIL, which is top 3 biggest assembly house in the world.
- PD&RD, Quality, & Sales, 5 years, Amkor Taiwan(Bumping)

- Vice Chairman of SEMI Taiwan PKG&TEST Committee.
- Chairman of TILA (Taiwan Intelligent Leader Association).
- Published more than 30 technical papers and granted more than 15 issued worldwide Patents.

Invited presentation 4: UV Laser Releasable Temporary Bonding Materials for Advanced Packaging technologies by Kenzo Ohkita, Ph.D.

JSR Corporation, Yokkaichi, Mie, Japan, kenzou_ookita@jsr.co.jp

ABSTRACT:

As Moore's law is reaching its limitations, the innovative evolutions of advanced electronic packages are required. Semiconductor devices that deploy 2.5D/3D integration and fan-out packages have progressed to satisfy these requirements in the recent decade. For 3D packaging, device wafers are usually thinned down to less than 100 μm for reducing total packaging thickness and the electrical resistance. On the other hand, for fan-out packaging manufacturing, silicon or glass support wafers are necessary as temporary substrates for building up re-distribution layers (RDLs) or for fabricating chip embedded mold wafers.

Temporary bonding (TB) technology is essential for realizing such high performance electronic packages. In this technology, the thin and fragile silicon wafers or fan-out wafer level packages (FO-WLPs) are enabled to be handled by fixing onto a rigid carrier. To release the wafers from the carrier, a UV laser release system is used and its process is very promising because of high-throughput manufacturing without mechanical stress at room temperature. The UV lase with highly energy density has advantages in terms of low heat damage and can directly induce photochemical reaction of carbon-carbon covalent bonds within the order of a nanosecond. The UV Laser release system also provide wider process window relative to the other releasing methods. This technology can be applied not only for silicon or mold wafers but also for large substrates in panels form.

In this presentation, an appropriate design for a material-pair which is adhesive and releaser layer used in temporary bonding process will be described. The material-pair should survive exposure to various chemical and thermal stresses through photolithography, electroplating, vapor deposition, and etching process. The adhesive with high rigidity at high temperature to support and protect device wafer is necessary. The release layer with high UV laser absorption rate to give selective decomposition of TB layer and low transmittance rate to minimize the potential damage to the device wafer are exhibited. Also, the chemical resistance and thermal resistance at 250 ^{o}C or even higher are required to apply the wide spread of device applications.

Bio: Dr. Kenzo Ohkita is a manager of Advanced Electronic Materials Laboratory at JSR Corporation. He is currently responsible for material development for 3D packaging technology, especially temporary bonding / debonding (TBDB) materials and photo-definable dielectrics. He received PhD in Chemistry at Osaka University (Japan, 1994). After joining JSR, he has 20 years' experience in research and development of various materials; functional polymers design and their large volume production, high heat-resistant resins, photoresist for display applications, and materials for printed electronics applications.

Invited presentation 5: Trends in SIP and Placement Approaches

Abstract: Advance Packaging has been evolving through the utilization of various packaging technologies. Driving small package through innovation and miniaturization will help respond to the market faster. One of the key examples is the increase of the use of SIP packages (System-in-package). One of the trends of SIP is the increase use of multi chip and passives into a single package. This will help to drive lower cost in packaging at the same time add more functionality. The trends of adding even more I/O densities and complex integration in a smaller form factor has given SIP a flavor of Fan out wafer packaging technologies. A hybrid solution for placement approaches combining passives and die from a single platform not only potential reduces a second reflow in the process but address increase yield and less variety in the process. This presentation will also introduce advanced SIP packaging technologies with a thin substrate, thin die and integrated passive devices. They Hybrid is capable of handling a multiple of challenges to address the trends of SIP.

Bio: **Chong Chan Pin** Senior Vice President, AP-Hybrid, Electronics Assembly, Wedge Bonders, Capillaries and Blades
Business Lines
Chan Pin was appointed as Senior Vice President of K&S's AP-Hybrid, Electronics Assembly, Wedge Bonders and Consumables Business Lines in December 2016. He joined K&S in 2014 as Vice President of Wedge Bonders business group and has successfully turnaround the business and led the team to higher growth by diversifying the business into the battery bonding market.
Chan Pin is a technology industry veteran with more than 24 years of engineering and operations experience in the semiconductor and electronics industry. He started his career first as a Process and Test Engineer at Motorola Pagers and Cellular group and pioneered multiple factories in Asia before advancing to the role of Manufacturing Manager at Flextronics. In

1999, Chan Pin joined KLA-Tencor and held a number of diverse positions, including Senior Technical Director of Engineering and General Manager of Strategic Business Unit in Greater China. Chan Pin then pioneered the efforts of starting the MEMS factory in Singapore when he became the Vice President of Sales and General Manager at Form Factor. Most recently, he was the Global President & CEO at Everett Charles Technologies, managing and leading in test and probe technologies.
Chan Pin received his bachelor's degree in Electrical Engineering and Computer Science from the State University of New York at Buffalo and a master's degree in Business Administration from the University of Leicester, United Kingdom. A Singaporean national, he is a military reserve (National Service, NS) Brigade 2nd in Command of a combined arms division.

Invited presentation 6: Wafer Bonding – An Enabling Technology for 3DIC, MEMS, BSI CIS, SOI, RF Filters, and More

Abstract:

Wafer bonding is one of the enabling technology for most 3DICs (3D Integrated Circuits), MEMS (Micro Electro Mechanical Systems), MOEMS (Micro Optical Electro Mechanical Systems), BSI (Back Side Illuminated Image Sensor), CIS (CMOS Image Sensors), SOI wafers, heterogeneous integration, multi junction PV (Photo Voltaic) cells, high performance RF (Radio Frequency) filters, microfluidics and wafer level optics. This presentation will highlight the often hidden process of wafer bonding by reviewing the primary aligned wafer bonding processes for 3DICs, MEMS, BSI CIS, and heterogeneous integration. The bonding processes reviewed will include direct bonding, plasma activated direct bonding, hybrid bonding, solder/ eutectic bonding, and thermo-compression bonding.

Bio: Eric Pabo is the Business Development Manager for MEMS for EV Group, prior to this he was the Bonding Applications Engineer for EV Group in North America. He has been with EV Group for over 11 years, has 34 years of experience in electronics manufacturing, with 18 years of experience in wafer bonding and wafer level packaging at Hewlett Packard, Agilent Technologies and EV Group.

Eric is a registered Professional Engineer in the state of Colorado, is a Six Sigma Black Belt and has a Mechanical Engineering Degree from Colorado State University.

Eric occupies any spare time he may have with his hobby of photography.

Invited presentation 7: VCSEL-based Optical Interconnects and Their Packaging Technologies

By Hideyuki Nasu, Furukawa Electric Co., Ltd.

Abstract:

Optical interconnects have been widely deployed to rack-to-rack connections in high speed data transmission systems as increasing an information capacity in data centers and improving a processing capacity of high performance computing. It has been expected that a demand to adopt optical interconnects keeps growing further. VCSELs have been a major light source in conventional short reach optical communication systems. Consecutively, newly commercialized 25-Gb/s VCSELs initiated the actual usage in systems. As a practical result, Broadcom reported that the latest total shipment volume of 25-Gb/s VCSELs already reached more than 1 million. For 100-Gb/s applications, QSFP28-based AOCs and transceivers have been employed for front panel connections. 25-Gb/s × 12-channel on-board optical modules for a higher-density packaging architecture are in a commercialization stage at present. To the next generation high capacity data transmission, various technical developments to realize a serial data rate of >50 Gb/s have been in progress. This presentation gives the recent progress and future prospect on VCSEL-based optical interconnects and their packaging technologies.

Biography:

Hideyuki Nasu received the B.E., M.E., and Ph.D. degrees from the College of Science and Technology, Nihon University, Tokyo, Japan, in 1993, 1995, and 2006, respectively. In 1995, he joined Furukawa Electric Co. Ltd., Tokyo, Japan. He has worked for development and commercialization of parallel-optical modules for optical interconnects. He is an author or coauthor of 55 patents and more than 100 publications.

Dr. Nasu is a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE), the Mission Fellow of the Japan Institute of Electronics Packaging (JIEP), and a Member of the Information and Communication Engineer (IEICE) of Japan. He has served the Vice Chair of the Optical Packaging Technology committee of JIEP since 2016. He has also served the Optoelectronics Field Chair of IEEE CPMT Symposium Japan (ICSJ) since 2015 and the Program Chair since 2017. He received the Technology Award in 2012 and the Best Conference Paper Award in 2016 from JIEP, and the Best Paper Award from ICSJ in 2016.

Invited presentation 8: Temporary Bonding Materials for Fan-out Packaging Processes

Abstract: Temporary bonding technology has been a fundamental enabler of ultra thin chips and chip packages for more than a decade now but the advanced packaging landscape is changing constantly to keep up with increasing demands from electronics designers and consumers for high density integration, better performance and reduction in form factor. Carrier-assisted wafer handling using a temporary bonding material has also evolved to keep pace with the developments in advanced packaging.

Earlier in the development of the temporary bonding materials, most of the material requirements were driven by the need to mechanically support ultrathin and stress-prone silicon and compound semiconductor wafers to enable through silicon via or interposer fabrication on the wafer-fab side. Now, with the evolution of fan-out wafer level and panel level packages, the attention is focused on the chip packaging side for fan-out processes. Although there are still some fundamental similarities in the process of bonding and debonding of the device substrates, the requirements for the temporary bonding materials have vastly changed to accommodate the various architectures and process flows involved in fan-out technology.

For TSV fabrication in the wafer fab side, the temporary bonding materials evolved from waxes to thermoplastic adhesives to accommodate the stress of the wafer and temperature requirements of the process. Now, we have introduced advanced multi-layer materials combining thermoplastic and curable materials for handling increased stress and CTE mismatch typically observed in a reconstituted wafer used in fan-out processes. The materials

can also withstand much higher temperatures (up to 350°C) and provide a mechanically stable platform for processing the device substrate. Moreover, we have developed new generation of laser release materials to address the challenges faced in build-up approaches used for RDL-first fan-out processing.

This presentation will illuminate the advancements and challenges in material and process technology to support the new chip-first and RDL-first fan-out architectures for both wafer-level and panel-level fan-out manufacturing.

Bio: Ram Trichur is the Director of Business Development at Brewer Science. In his current role, he oversees world-wide business development for advanced packaging materials. He received his B.Engg degree in Electrical Engineering from Bharathidasan University, India and his M.S degree in Electrical Engineering from University of Cincinnati. He has received 3 patents and is the author of more than 30 publications. Prior to joining Brewer Science he was a microfluidics research engineer at Bruker Corporation in Billerica, MA.

Invited presentation 9: On-Chip Embedded Cooling of Power and Logic Components

by Avram Bar-Cohen, PhD, IEEE/EPS President Elect (2018-2019)
Principal Engineering Fellow, Raytheon Corporation – Space & Air Borne Systems, Rosslyn, Virginia, USA

ABSTRACT:

- Thermal packaging technology has been a key enabler in the development of today's microelectronic systems and is responsible for much of the benefit that we derive from miniaturization, higher performance, lower cost and greater reliability of today's electronic "widgets." A review of thermal packaging over the first 70 years of the Information Age will reveal a relentless "inward migration" of cooling technology from room ventilation and air-conditioning, to cabinet cooling, to component cooling with heat sinks and cold plates, and to today's efforts to address on-chip hot spots and near-junction thermal transport. Attention will then be devoted to a discussion of Gen3 thermal management technologies relying on intra- and interchip microfluidic cooling, use of diamond substrates, and on-chip thermoelectric coolers to implement the emerging "embedded cooling" paradigm.

Bio: Dr. Avram Bar-Cohen is an internationally recognized leader in thermal science and technology, an Honorary Member of ASME and Life Fellow of IEEE, currently serving as a Principal Engineering Fellow at Raytheon Corporation – Space and Airborne Systems, on leave from the University of Maryland. His publications, lectures, short courses, and research, as well as his US government and Professional service in ASME and IEEE, have helped to create the scientific foundation for the thermal management of electronic components and systems. His current efforts focus on embedded cooling, including on-chip thermoelectrics, diamond substrates, and two-phase microchannel coolers for high heat flux electronic and photonic components in computational, radar, and directed energy systems.

Bar-Cohen is a former Editor-in-Chief of the IEEE CPMT Transactions and serves on the Board of Governors of the CPMT Society. He has represented the Society as a Distinguished Lecturer for more than 15 years and is the President-elect of the CPMT Society. He recently completed his service as a Program Manager in the Microsystem Technology Office at the Defense Advanced Projects Agency in Virginia and had earlier served as Department Chair of Mechanical Engineering and Distinguished University Professor at the University of Maryland – College Park.

In 2014 Bar-Cohen was honored by the IEEE with the prestigious CPMT Field Award and had earlier been recognized with the CPMT Society's Outstanding Sustained Technical Contributions Award (2002). Among other awards, Bar-Cohen received the Luikov Medal from the International Center for Heat and Mass Transfer in Turkey (2008) and ASME's Heat Transfer Memorial Award (1999), Edwin F. Church Medal (1994), and Worcester Reed Warner Medal (1990).

In addition to serving as the Editor-in-Chief of WSPC's Encyclopedia of Thermal Packaging and the co-editor of the *Advanced Integration and Packaging* book series, Bar-Cohen has co-authored Dielectric Liquid Cooling of Immersed Components (WSPC, 2013), Design and Analysis of Heat Sinks (Wiley, 1995), and Thermal Analysis and Control of Electronic Equipment (McGraw-Hill, 1983), and has edited/co-edited 28 other books in this field. He has authored/co-authored more than 400 journal papers, refereed proceedings papers, and

chapters in books and has delivered some 100 keynote, plenary and invited lectures at major Conferences, Symposia, and college campuses throughout the world.

Picture:

Invited presentation 10: Reliability Assurance: A Semiconductor Supplier's Perspective

By Stevan G. Hunter

This presentation will explore and highlight the current reliability space from the perspective of the semiconductor supplier. Semiconductor components and ICs have generally had good reliability lifetimes, and manufacturers are still driven in their relentless efforts to eliminate defects to improve yield and reliability. The concepts of Design for "X" (DfX) are easier said than done in the supplier's cost- and schedule-constrained environment. Reliability test and qualifications costs, schedule, and effectiveness are continually being scrutinized due to increasing customer expectations and more stringent industry standards. Lean six sigma practices are widespread in semiconductor manufacturing. Semiconductor reliability improvements are typically made by "guardbanding" or tightening process or test limits, not through a fundamental improvement that eliminates the "physics of failure". Field returns data is important, but often difficult to obtain in sufficient detail, and is clouded with processing by the sequence of customers after parts are out of the semiconductor supplier's control. Customers have the responsibility to preserve the built-in reliability of semiconductors, especially by preventing EOS and ESD in their operations. The risks of previously unknown or untested "physics of failure" mechanisms increase as devices continue to shrink, new processes are introduced, and integration escalates with 3-D packaging.

BiO: Stevan G. Hunter, PhD, is a Member of Technical Staff, for Quality and Reliability, at ON Semiconductor, Phoenix, AZ. He has 39 years semiconductor industry experience, teaches Lean Six Sigma courses at ON, teaches at BYU-Idaho and Arizona State University as adjunct, and is an adjunct faculty member at the University of Maryland CALCE. Stevan holds certifications as Six Sigma Blackbelt, Reliability Engineer, and ESD Factory Control Manager. He is a Senior Member of IEEE and ASQ, member of IMAPS, and serves on the EOS/ESD Association Industry Council and various committees.

Invited presentation 11: Advanced eWLB FOWLP: Enabling Integrated Packaging Solutions

Seung Wook Yoon, Ph.D, STATS ChipPAC Ltd. 10 Ang Mo Kio Street 65 Techpoint #04-08/09 Singapore 569059, Seungwook.yoon@statschppac.com

ABSTRACT: New and emerging applications in the consumer and mobile space, the growing impact of the automotive, Internet of Things (IoT) and wearable electronics (WE) and the complexities in sustaining Moore's Law have been driving many new trends and innovations in advanced packaging technology. And the advancement of silicon scaling to 7/10 nanometer (nm) in support of higher performance, bandwidth and power efficiency in mobile devices is pushing the boundaries of emerging packaging technologies to smaller packaging designs with finer line/spacing as well as improved electrical performance and highly integration. Advanced embedded Wafer Level Ball Grid Array (eWLB) technology provides a versatile platform for the semiconductor industry's technology evolution from single or multi-die 2D package designs to 2.5D interposers and 3D System-in-Package (SiP) configurations.

This paper reports developments that advanced eWLB FOWLP technology, including integration of multi-die, discretes, embedded passives and crystals. This will also discuss the adoptions and new features available for automotive, mobile, IoT and WE. This advanced technology is well designed for MEMS/sensors SiP modules as well as thin, highly integrated packaging. Innovative 2.5D/3D packaging features will be also introduced with the merits and characterization data for specific applications.

Various test vehicles have been designed and fabricated to demonstrate these low profile solutions for mobile, portable and wearable electronics. The test vehicles have ranged from medium to large sizes and 0.4mm bottom ball pitch. To enable higher interconnection density and signal routing, packages with multi layer redistribution (RDL) and fine line/width spacing are fabricated and implemented on the eWLB platform. Successful reliability characterization results are reported as an enabling technology for highly integrated miniaturized, low profile and cost-effective solutions.

Bio: Dr. YOON is currently working as director of Advanced Products & Technology Marketing, STATS ChipPAC Pte. Ltd in Singapore. His major interests are for Advanced Packaging and Integration Technology including eWLB/Fanout WLP, SiP and integrated 3D IC packaging.

Prior to joining STATS CHIPPAC LTD, He was deputy lab director of MMC (Microsystem, Module and Components) lab, IME (Institute of Microelectronics), A*STAR, Singapore. ”YOON” received Ph.D degree in Materials Science and Engineering from KAIST, Korea. He also holds MBA degree from Nanyang Business School, Singapore. He has over 250 journal papers, conference papers and trade journal papers, and over 20 US patents on microelectronic materials and electronic packaging. Currently working as technical committee member of various international packaging technology conferences, EPTC, ESTC, iMAPS, IWLPC and SEMI.

Invited presentation 12: Highly accurate TSV, PWB and FO-PLP wirring fabication by plasma dry processes for interface.
By Yasuhiro Morikawa

Abstract
High-performance CPU and large capacity memory for AI / DL, edge- computing and high density packaging technology, are indispensable to realize the next-generation IoT cloud society. High-density packaging technologies such as 3D-IC, 2.5 / 2.1D and 2D scheme basing on PCB (Print Circuit Board) substrate are among key technologies to satisfy the requirements from the both smart semiconductor devices and smart functional devices such as heterogeneous integration. ULVAC has been continuously developing manufacturing solutions for TSV, Embedding and Fan-Out (PWB, WLP / PLP) packaging. In this presentation, buildup multilayer, RDL, TSV technologies solutions consisting of plasma etching / ashing and PVD (Physical Vapor Deposition) sputtering to make the high density interconnection package will be introduced.

Bio: Yasuhiro Morikawa" is currently the manager of development of dry etching / ashing and polymer coating technologies for 2D, 2.5D, and 3D packaging applications within the Institute of Semiconductor and Electronics Technologies at ULVAC. And, he has been also development for the deep quartz etcher for Opt and Bio-MEMS applications.

Yasuhiro joined ULVAC in 1997. He earned his Master. in Electrical engineering from the University of Toyo in 1997. And, he received a Ph.D. in Material Engineering from the University of Tokyo in 2003.

Yasuhiro is a member of the Japan Society of Applied Physics, Committee of International Symposium on Dry Process (DPS) , and Member of The Japan Institute of Electronics Packaging(JIEP)

Invited presentation 13: 10 Golden Rules of Chip- Package- Board Interactions

By E.Napetschnig, Infineon Technologies Austria AG ; Villach Austria

Abstract: As they strive to reach even better technology solutions in even faster time the semiconductor industry engineers of today tend to forget about basic principles. The ten golden rules aim to support the engineers to find the best solution by questioning the right way. As the rules are very basic every engineer in the semiconductor industry can apply them. Most experienced technical experts have come together and formulated the rules, thus, best results are granted as the worst failure paths are included. The most experienced engineers of Infineon Technologies AG came together and formulated the rules to enable a faster time to market while implementing highly reliable stable processes in the end. On the first sight some of the rules are very basic technical common sense, but too often the basic principles are overseen during project planning and will lead to issues, delays and even fail and cancelation of the projects. This list of ten golden rules can be print out on one sheet, placed on every table of a semiconductor engineer and can act as a reminder to respect the most basic principles of material science, mechanics, thermodynamics and electronics while keeping an eye on the productivity. Omitting the 10 golden rules is helping to decrease the complexity of the available process and thus allow approaching the highest quality requirements that are given by the current market.

Bio: Evelyn Napetschning received her Ph.D. and Masters degrees in Technical Physics from Vienna University of Technology, Austria in 2008 and 2003 respectively. Dr. Evelyn has 11 years of experience in semiconductors frontend/backend process integration. She is currently a Senior Staff Engineer at Infineon Technologies. She is also holding Process Block Catalogue Integration Champion and Complexity Manager position within the TEX complexity management team, Villach. Dr. Evelyn holds 7 patents to her credit.

Invited presentation 14: Heterogeneous Integration Roadmap – Global Collaboration

BY William Chen, ASE Group

The electronic industry has reinvented itself through multiple disruptive changes in market, business, and technologies. We are now entering a new era of digital economy with data migration to the cloud, smart devices everywhere, Internet of Things to Internet of Everything, and the emergence of autonomous vehicles. While Moore's Law is slowing, the pace of technology innovation continues to expand to meet challenges of the new era. The crucial question is: how do we re-invent the Technology Roadmap and chart the critical paths going forward?

The IEEE Electronic Packaging Society (EPS), Electron Devices Society (EDS), and Photonics Societies, ASME EPPD and SEMI have joined in collaboration to re-invent the Technology Roadmap for the professional, industry, academia and research communities. The Heterogeneous Integration Roadmap (HIR) will follow directly the purpose, process and format of the ITRS for the 15-year assessment of future requirement, and 25-year assessment for emerging materials and emerging devices. The roadmap will address disruptive changes in the market place, major challenges in technology requirements, while identifying roadblocks and potential solutions. The goal is to stimulate research to address the roadblocks and to realize the potential solutions.

This talk will report on the disruptive market landscape, examples of heterogeneous integration innovations, followed by the global roadmap collaboration in the making of the Heterogeneous Integration Roadmap. We shall introduce the work of the Technical Working Groups in achieving the purpose to provide long term vision into the future and identifying the needs of future system applications.

Bio: William Chen (Bill) holds the position of ASE Fellow and Senior Technical Advisor at ASE Group . Prior to joining the ASE, he was the Director at the Institute of Materials Research & Engineering in Singapore. He retired from IBM Corporation after over thirty years in various technical & management positions. He has held adjunct and visiting faculty positions at Cornell University, Hong Kong University of Science and Technology, and Binghamton University. He was a past President of the IEEE CPMT Society. He has been elected a Fellow of IEEE and a Fellow of ASME. He chairs the IEEE Heterogeneous

Integration Roadmap initiative. He received B. Sc from London University, M.Sc from Brown University and PhD from Cornell University.

Invited presentation 15: Interconnect Reliability Assurance Through Electrical Testing

By Cher Ming Tan, Director, Center for Reliability Sciences and Technologies, Chang Gung University, Taiwan

Abstract: Interconnect is an essential part of IC packaging. Basically, the two main type of interconnects are wire bonding and solder. Failure of wire bonding over time can be due to prolonged temperature and/or power cycling and hence accelerated cycling test are usually performed to assure its reliability. However, in-situ temperature or power cycle test to determine the on-set of wire failure is currently not possible. An electrical method is developed where a continuous monitoring of bonding wire integrity during accelerated temperature or power cycling test become possible, and will be presented in this talk.

Another aspect of bonding wire is the pull strength to assure its quality. Pull strength can be degraded either due to bond failure and wire failure. While bond failure can be related to wire bonding process parameter and the cleanliness of the bondpad, wire failure is related to the wire itself, although wire bonding process can also induce wire failure due to the HAZ. Generally, the analysis of pull strength is simply based on the failure strength, but the separation of the above-mentioned two mechanisms are necessary as their corrective actions will be different. This talk will present a method to analyze the pull strength data with example to illustrate this method.

Bio: Dr. Tan received his Ph.D in Electrical Engineering from the University of Toronto in 1992. He has 10 years of working experiences in reliability in electronic industry (both Singapore and Taiwan) before joining Nanyang Technological University (NTU) as faculty member in 1996 till 2014. He joined Chang Gung University, Taiwan and set up a research Center on Reliability Sciences and Technologies in Taiwan and acts as Center Director. He is Professor in Electronic Department of Chang Gung University, Honorary Chair Professor in Ming Chi University of Technology, Taiwan. He has published more than 300 International Journal and Conference papers, and giving 10 keynote talks and 50 invited talks in International Conferences and several tutorials in International Conferences. He holds 12 patents and 1 copyright on reliability software. He has written 4 books and 3 book chapters in the field of reliability. He is an Editor of Scientific Report, Nature Publishing Group, an Editor of IEEE TDMR and Series Editor of SpringerBrief in Reliability. He is a member of

the advisory panel of Elsevier Publishing Group. He is also in the Technical committee of IEEE IRPS.

He is a past chair of IEEE Singapore Section, senior member of IEEE and ASQ, Distinguish Lecturer of IEEE Electronic Device Society on reliability, Founding Chair and current Chair of IEEE Nanotechnology Chapter - Singapore Section, Fellow of Institute of Engineers, Singapore, and Fellow of Singapore Quality Institute. He is the Founding Chair of IEEE International Conference on Nanoelectronics, General Chair of ANQ Congress 2014. He is also the recipient of IEEE Region 10 Outstanding Volunteer Award in 2011. He is Guest Editor of International J. of Nanotechnology, Nano-research letter and Microelectronic Reliability. He is in the reviewer board of several International Journals such as Thin Solid Film, Microelectronic Reliability, various IEEE Transactions, Reliability Engineering and System Safety etc for more than 5 years. He is the only individual recipient of Ishikawa-Kano Quality Award in Singapore since 2014. He is also current active in providing consultation to multi-national corporations on reliability.

His research interests include reliability and failure physics modeling of electronic components and systems, finite element modeling of materials degradation, statistical modeling of engineering systems, nano-materials and devices reliability, and prognosis & health management of engineering system.