Conference Program

- All events are held at the Grand Copthorne Waterfront Hotel, Singapore, unless otherwise stated.
- This Conference Program is subjected to changes (confirmation of the breakout sessions is subjected to the authors' registration and payment)

Wednesday, 6th December 2017	
7:00am - 8:30am	**PDC Registration** @ Flamingo room, Level 3
8:30am - 12:00pm	**Professional Development Courses** **1. Electronic Packaging for 5G Microwave and Millimeter Wave Systems IEEE** @ Paradiso Room **- Dr. Rick Sturdivant** **2. Automotive electronics – requirements and reliability** @ Cardinal Room **- Dr. Mervi Paulasto-Kröckel** **3. MEMS Fabrication: from theory to packaging** @ Swallow Room **- Dr. Liu Aiqun**
12:00pm - 1:30pm	**Lunch** @ Galleria Foyer, Level 3
1:30pm - 5:00pm	**Professional Development Courses** **4. Fan-Out Wafer-Level Packaging and 3D Packaging** @ Paradiso Room **- Dr. John H Lau** **5. Reliability from a Semiconductor Suppliers Perspective** @ Cardinal Room **- Dr. Stevan Hunter** **6. Advanced LED packaging technology and reliability** @ Swallow Room **- Dr. Ricky Lee**
5:30pm - 7:30pm	**Panel Session** @ Galleria Ballroom, Level 3 **Packaging Challenges & Opportunities of 5G-mm Wave Technology**
7:30pm - 10:00pm	**Dinner: VIP**

Thursday, 7th December 2017	
7:45am - 8:30am	**Conference Day 1 Registration** @ Flamingo room, Level 3
8:30am - 9:00am	**Welcome and opening speech** @ Grand Ballroom, Level 4
9:00am - 9:30am	**Keynote speech 1** @ Grand Ballroom, Level 4 **Extending Moore's Law with Advanced Packages** **- W.K.Wong(Xilinx)**
9:30am - 10:00am	**Keynote speech 2** @ Grand Ballroom, Level 4 **The evolution of packaging technology for mobile platform - Where we have been and where we are headed** **- Dr. Raj Pendse (Qualcomm)**
10:00am - 10:30am	**Coffee/ Tea Break #1** **Interactive Session #1** @ Foyer of Grand Ballroom II, Level 4
10:30am - 11:50pm	**Technical Session A (5 tracks)** **S-01: TSV/Wafer Level Packaging** @ Paradiso Room **S-02: Interconnection Technologies** @ Cardinal Room **S-03: Material and Processing** @ Swallow Room **S-04: Mechanical modeling & simulation** @ Lyrebird Room **S-05: Quality, Reliability & FA** @ Falcon Room
11:50pm - 1:20pm	**Lunch** @ Grand Ballroom, Level 4 **EPTC 2016 Best Paper Awards** **EPTC 2017 Organizing Committee Appreciation**
1:20pm - 1:50pm	**Invited Presentation** **01: Enhanced Bonding Technology for Hybrid Integration in 3D Packaging Technology** @ Paradiso Room **02: Packaging of Integrated Silicon Photonics devices : Electrical, Optical, Thermal Challenges and Application** @ Cardinal Room **03: Innovative Process and Equipment Technology Solutions for 3D SiP Packaging** @ Swallow Room **04: UV Laser Releasable Temporary Bonding Materials for Advanced Packaging technologies** @ Lyrebird Room **05: Trends in SIP and Placement Approaches** @ Falcon Room
1:50pm - 3:10pm	**Technical Session B (5 tracks)** **S-06: Advanced packaging** @ Paradiso Room **S-07: Emerging Technologies** @ Cardinal Room **S-08: Equipment and Process automation** @ Swallow Room **S-09: Material and Processing** @ Lyrebird Room **S-10: Interconnection Technologies** @ Falcon Room

3:10pm - 4:30pm	**Coffee/Tea Breaks #2** **Exhibitor Presentation** @ Grand Ballroom, Level 4.
4:30pm - 5:50pm	**Technical Session C (5 tracks)** **S-11: Mechanical modeling & simulation** @ Paradiso Room **S-12: Quality, Reliability & FA** @ Cardinal Room **S-13: Thermal Characterization & cooling solutions** @ Swallow Room **S-14: Emerging Technologies** @ Lyrebird Room **S-15: Electrical Simulation & Characterization** @ Falcon Room
6:30pm - 10:00pm	**Conference Banquet**

Friday, 8th December 2017	
8:30am - 9:00am	**Invited Presentation** **06: Wafer Bonding – An Enabling Technology for 3DIC, MEMS, BSI CIS, SOI, RF Filters, and More** @ Paradiso Room **07: VCSEL-based Optical Interconnects and Their Packaging Technologies** @ Cardinal Room **08: Temporary Bonding Materials for Fan-out Packaging Processes** @ Swallow Room **09: On-Chip Embedded Cooling of Power and Logic Components** @ Lyrebird Room **10: Reliability Assurance: A Semiconductor Supplier's Perspective** @ Falcon Room
9:00am - 10:20am	**Technical Session D (5 tracks)** **S-16: Interconnection Technologies** @ Paradiso Room **S-17: Emerging Technologies** @ Cardinal Room **S-18: Material and Processing** @ Swallow Room **S-19: Thermal Characterization & cooling solutions** @ Lyrebird Room **S-20: Quality, Reliability & FA** @ Falcon Room
10:20am - 11:10am	**Coffee/Tea Breaks #3** **Exhibitor Presentation** @ Grand Ballroom, Level 4
11:10am - 12:30pm	**Technical Session E (5 tracks)** **S-21: Materials and Processing** @ Paradiso Room **S-22: Advanced Packaging** @ Cardinal Room **S-23: TSV/Wafer Level Packaging** @ Swallow Room **S-24: Electrical Simulations & Characterization** @ Lyrebird Room **S-25: Mechanical Modeling & Simulations** @ Falcon Room

12:30pm - 1:30pm	**Lunch** @ Grand Ballroom, Level 4 **Introduction of 20th Electronic Packaging Technology Conference**
1:30pm - 2:00pm	**Invited Presentation** **11: Advanced eWLB FOWLP: Enabling Integrated Packaging Solutions** @ Paradiso Room **12: Highly accurate TSV, PWB and FO-PLP wiring fabication by plasma dry processes for interface** @ Cardinal Room **13: 10 Golden Rules of Chip- Package- Board Interactions** @ Swallow Room **14: Heterogeneous Integration Roadmap - Global Collaboration** @ Lyrebird Room **15: Interconnect Reliability Assurance Through Electrical Testing** @ Falcon Room
2:00pm - 3:20pm	**Technical Session G (5 tracks)** **S-26: Advanced Packaging** @ Paradiso Room **S-27: TSV/Wafer Level Packaging** @ Cardinal Room **S-28: Interconnection Technologies** @ Swallow Room **S-29: Emerging Technologies** @ Lyrebird Room **S-30: Electrical Simulations & Characterization** @ Falcon Room
3:20pm - 3:50pm	**Coffee/Tea Break #04** **Interactive session #2** @ Foyer of Grand Ballroom II
3:50pm - 4:20pm	**Keynote speech 3** @ Grand Ballroom, Level 4 **Design tools and modelling for power electronics packages – current status and future challenges** **- Prof. Bailey(University of Greenwich)**
4:20pm - 4:40pm	**Closing Ceremony: Lucky Draw**

Saturday, 9th December 2017	
8:30am - 12:00pm	**Institution Visit - URA smart city Gallery**

Technical Sessions A

Thursday, 7th December 2017, 10:30am - 12:10pm

Technical Session S-01: TSV/Wafer Level Packaging Chair: **Avram Bar-Cohen** Room: Paradiso Room	
10:30am	**A-01: ID 283 - 3D Si Interposer & WLP for Small Power Devices for Harsh Conditions** Author(s) - Jean Charbonnier[1], Aurélia Plihon[1], Myriam Assous[1], Maxime Argoud[1], Nacima Allouti[1], Stéphane Moreau[1], Nadine David[1], Catherine Brunet-Maquat[1], Christian Hartler[2], Joerg Siegert[2], Ewald Wachmann[2] *1. CEA Leti, France* *2. ams AG, Austria* *jean.charbonnier@cea.fr*
10:50am	**A-06: ID 190 - Novel ICP Plasma Etching for Backside TSV.** Author(s) - Toshiyuki Sakuishi, Takahide Murayama, Yasuhiro Morikaw *ULVAC,Inc., Japan; toshiyuki_sakuishi@ulvac.com*
11:10am	**A-11: ID 256 - The adhesion study of back-side dielectric film within 3D process integration** Author(s) - Hongyu Li *IME, Singapore; lihy@ime.a-star.edu.sg*
11:30am	**A-16: ID 300 - Carrier-Based Linear Transport PVD System Results for RDL Barrier/Seed Deposition in Fan-Out Packaging Applications** Author(s) - Paul Francis Werbaneth, Terry Bluck, Chun-Chung Chen, Daniel Gallagher, Vladimir Kudriavstev, Lisa Mandrell, Billy Runstadler, Chris Smit *Intevac, Inc., United States of America* *pwerbaneth@intevac.com*

Technical Session S-02: Interconnection Technologies Chair: **Thomas Zerna** Room: Cardinal Room	
10:30am	**A-02: ID 169 - Visualization of Oxide Removal during Ultrasonic Wire Bonding Process** Author(s) - Yangyang Long[1], Folke Dencker[2], Andreas Isaak[2], Friedrich Schneider[3], Jörg Hermsdorf[3], Marc Wurz[2], Jens Twiefel[1] *1. Institute of Dynamics and Vibration Research, Leibniz Universität Hannover, Germany* *2. Institute of Micro Production Technology, Leibniz Universität Hannover, Germany* *3. Laser Zentrum Hannover e.V., Germany* *long@ids.uni-hannover.de*
10:50am	**A-07: ID 203 - Towards Reliable 10µm Pitch Assembly Using Cu/Ni/SnAg based Interconnects** Author(s) - Divya Taneja[1,2], Marion Volpert[1], Tarik Chaira[1], David Henry[1], Fiqiri Hodaj[2] *1. CEA-LETI, France* *2. University Grenoble Alpes, SIMAP* *divya.taneja@cea.fr*

11:10am	**A-12: ID 246 - Feasability Study of Piezo Jet Printed Silver Ink Structures for Interconnection and Condition Monitoring of Power Electronics Components** Author(s) - Martin Mueller, Joerg Franke *University Erlangen-Nuremberg, Germany; martin.mueller@faps.fau.de*
11:30am	**A-17: ID 205 - Improvement of Lifetime Prediction of Silver Sintered Material in Automotive Power Devices** Author(s) - Ryosuke YAEJIMA[1], Shota OKUNO[1], Qiang YU[1], Yusuke NAKATA[2], Hiroyuki SUGAWARA[2] *1. Yokohama National University, Japan* *2. Calsonic Kansei Co.,Ltd, Japan* *yaejima-ryosuke-mn@ynu.jp*

Technical Session S-03: Materials and Processing Chair: **Sungdong Kim** Room: Swallow Room	
10:30am	**A-03: ID 127 - The Correlation between Sintered Silver Joint Reliability and Pressure Assisted Sintering Parameters** Author(s) - Wayne Chee Weng Ng[1], Keith Sweatman[1], Kenji Takamura[1], Keisuke Kumagai[1], Takatoshi Nishimura[1], Sebastian Letz[2], Andreas Schletz[2] *1. Nihon Superior Co., Ltd., Osaka, Japans* *2. Fraunhofer IISB, Nuremberg, Germany* *wayne@nihonsuperior.co.jp*
10:50am	**A-08: ID 207 - Die Level 3D Heterogeneous Integration of a Microfluidic System** Author(s) - Pavani Vamsi Krishna Nittala, Prosenjit Sen *CeNSE, IISc Bangalore, India; vamsinittala@gmail.com*
11:10am	**A-13: ID 128 - Effect of rheological characterization on the jet printing performance of lead-free solder paste** Author(s) - Saipeng Li, Jian Hao, Shuang Tian, Dapeng Wang, Jian Zhou, Feng Xu *Southeast University, People's Republic of China; lisaipeng@seu.edu.cn*
11:30am	**A-18: ID 140 - Method for Assessing the Delamination Risk in BEoL Stacks around Copper TSV Applying Nanoindentation and Finite Element Simulation** Author(s) - Jan Albrecht[1], Marie Weissbach[1], Juergen Auersperg[1,2], Sven Rzepka[1] *1. Micro Materials Center at Fraunhofer ENAS, Germany* *2. Berliner Nanotest und Design GmbH, Germany* *jan.albrecht@enas.fraunhofer.de*

Technical Session S-04: Mechanical Modeling & Simulations Chair: **Christopher Bailey** Room: Lyrebird Room	
10:30am	**A-04: ID 119 - Larger FCBGA Package with Thin and Normal Core Evaluation and Characterization** Author(s) - Vito Lin, Nicholas Kao, Don Son Jian *SPIL, Taiwan; chichshenglin@spil.com.tw*
10:50am	**A-09: ID 188 - Non-contact Technology by Near-field Measurement** Author(s) - Ping Chia Su, Cheng-Dao Li, Sung-Mao Wu *National University of Kaohsiung, Taiwan, Taiwan; s7616989@gmail.com*
11:10am	**A-14: ID 137 - Thermo-mechanical Design of Fan-out Wafer Level Package for Power Converter Module** Author(s) - Zhaohui Chen *IME A-Star, Singapore; chenz@ime.a-star.edu.sg*
11:30am	**A-19: ID 167 - The life cycle impact assessment that the variabilities of BGA solder connection makes** Author(s) - Ryosuke Yano, Qiang YU *Yokohama National University, Japan; yano-ryosuke-tg@ynu.jp*

Technical Session S05: Quality, Reliability & Failure Analysis Chair: **Stevan G Hunter** Room: Falcon Room	
10:30am	**A-05: ID 154 - Review on test vehicles for electromigration (EM) study in solder interconnects** Author(s) - Ze Zhu[1], Yan-cheong Chan[1], Fengshun Wu[2], Chee Lip Gan[3], Zhong Chen[3] *1. City University of Hong Kong, Hong Kong S.A.R. (China)* *2. Huazhong University of Science and Technology, China* *3. Nanyang Technological University, China* *eeycchan@cityu.edu.hk*
10:50am	**A-10: ID 113 - Reliability Prediction of LED Packaging by Fatigue Behavior of Bonding Wire in Power Cycling Accelerated Test** Author(s) - Yongjun Pan[1], Fulong Zhu[1], Xinxin Lin[1], Fengren Wang[1], Lang Shi[1], Yan Kan[1], Sheng Liu[1,2] *1. School of Mechanical Science and Engineering, Huazhong University of Science and Technology, China* *2. School of Power and Mechanical Engineering, Wuhan University, China* *yongjun_pan@hust.edu.cn*
11:10am	**A-15: ID 123 - Reliability of wearable electronics - case of water proof tests on smartwatch of Xiaomi Mi Band 2** Author(s) - Yuk Ngang Zita Yip *City University of Hong Kong, Hong Kong S.A.R. (China); zitayip.yyn@my.cityu.edu.hk*
11:30am	**A-20: ID 165 - Optimization Of Chemistry For A Vapour Phase Process To Deflux No Clean Lead Free Materials On PCBs** Author(s) - Patrick J. Duchi, Jonathan Cetier, Laurent Levasseur, Jacquemine Coquio, Rodrigo Aguilar *Inventec Performance Chemicals; pduchi@inventec.dehon.com*

Technical Sessions B

Thursday, 7th December 2017, 1:50pm - 3:10pm

Technical Session S06: Advanced Packaging Chair: **Martin Oppermann** Room: Paradiso Room	
1:20pm	**Invited-01: Enhanced Bonding Technology for Hybrid Integration in 3D Packaging Technology:** Dr. Guilian Gao (Xperi)
1:50pm	**B-01: ID 286 - Full Wafer Redistribution and Wafer Embedding as Key Technologies for a Multi-Scale Neuromorphic Hardware Cluster** Author(s) - Kai Zoschke[1], Maurice Güttler[2], Lars Böttcher[1], Andreas Grübl[2], Dan Husmann[2], Johannes Schemmel[2], Karlheinz Meier[2], Oswin Ehrmann[3] *1. Fraunhofer IZM, Gustav-Meyer-Allee 25, 13355 Berlin, Germany* *2. Heidelberg University, Kirchhoff Institute for Physics, Im Neuenheimer Feld 227, 69120 Heidelberg* *3. Technical University of Berlin, Gustav-Meyer-Allee 25, 13355 Berlin, Germany* *kai.zoschke@izm.fraunhofer.de*
2:10pm	**B-06: ID 280 - Selective over-molding of a CMOS TSV wafer with the flexible 3D integration of components and sensors** Author(s) - Johan Hamelink *Boschman Technologies, Netherlands; johanhamelink@boschman.nl*
2:30pm	**B-11: ID 294 - Comprehensive Defect Monitoring Technique for Advanced Fanout Packaging Process** Author(s) - Vangal Aravindh[1], Richard Yeoh[1], Wesley Chang[2], ShihLin Pan[2], Wei Kuo[1], Anuj Pandey[1], Kevin Khoo[1], Rahul Lakhawat[1], Kootz Wang[1] *1. KLA Tencor (1 Technology Dr, Milpitas, CA 95035, USA)* *2. ASE (Lane 75, Waihuan West Road, Nanzi District, Kaohsiung City, Taiwan 811)* *Aravindh.Vangal@kla-tencor.com*
2:50pm	**B-16: ID 273- Enhancing magnetoelectric and optical properties of co-doped bismuth ferrite multiferroic nanostructures** Author(s) - Matin MD Abdul[1], Hossain M. N.[1], Mozahid F. A.[1], Islam M.R.[1], Rizvi M. H.[1], Hussain A.[1], Rahman M. M.[2], Islam M. F.[1] *1. Bangladesh University of Engg abd Tech (BUET), Bangladesh, People's Republic of;* *2. Ahsanullah University of Science and Tech (AUST)* *matin.md.a@gmail.com*

Technical Session S07: Emerging Technologies Chair: **Hideyuki Nasu** Room: Cardinal Room	
1:20pm	**Invited-02: Packaging of Integrated Silicon Photonics devices: Electrical, Optical, Thermal Challenges and Application:** Dr. Jun Su Lee (Tyndall National Institute)
1:50pm	**B-02: ID 121 - 128 x 128 Silicon Photonics MEMS Switch Package using Glass Interposer and Pitch Reducing Fibre Array** Author(s) - How Yuan Hwang *Tyndall National Institute, Ireland; howyuan.hwang@tyndall.ie*
2:10pm	**B-07: ID 282 - PUltra-Small Packaged Micro-Cooler for Medical Applications** Author(s) - José Miguel Fernandes[1], Pedro Anacleto[1], Luís Alexandre Rocha[1], João Gaspar[2], Paulo Mateus Mendes[1] *1. Universidade do Minho, Portugal* *2. International Iberian Nanotechnology Laboratory* *paulo.mendes@dei.uminho.pt*
2:30pm	**B-12: ID 141 - Molding Process Development for Low-Cost MEMS-WLCSP with Silicon Pillars and Cu Wires as Vertical Interconnections** Author(s) - Mian Zhi Ding, Boon Long Lau, Zhaohui Chen *Institute of Microelectronics, Singapore; dingmz@ime.a-star.edu.sg*
2:50pm	**B-17: ID 185 - Simulation Analysis of a Wearable Dry EEG Electrodes for Epilepsy Monitoring** Author(s) - Weiguo CHEN[1], Ramona DAMALERIO[1], Ruiqi LIM[1], Yuan GAO[1], Derrick CHAN[2], Ming-Yuan CHENG[1] *1. Institute of Microelectronics, Singapore* *2. KK Women's and Children's Hospital* *chenwg@ime.a-star.edu.sg*

Technical Session S08: Equipment and Process Automation Chair: **Eric Pabo** Room: Swallow Room	
1:20pm	**Invited-03: Innovative Process and Equipment Technology Solutions for 3D SiP Packaging:** Albert Lan (Applied Material)
1:50pm	**B-03: ID 172 - The Design of Near-Field Horizontal Probe Design for Wireless Charging Coil** Author(s) - Wang Tiang - An, Chen Bo - You, Wu Sung-Mao *National University of Kaohsiung, Taiwan; to0716@gmail.com*
2:10pm	**B-08: ID 206 - Indexer PVD Platform – The Key Enabler for High Productivity and Low Contact Resistance for Next-Generation WLP Applications** Author(s) - Patrik Carazzetti, Frantisek Balon, Mike Hoffmann, Juergen Weichart, Andreas Erhart, Ewald Strolz *Evatec AG, Switzerland; patrick.carazzetti@evatecnet.com*
2:30pm	**B-13: ID 301 - Investigations of Copper Wire Bonding Capability on Plasma Based Additive Copper Metallizations** Author(s) - Alexander Hensel[1], Klaus Kohlmann von Platen[2], Joerg Franke[1] *1. Institute for Factory Automation and Production Systems (FAPS)* *2. Friedrich-Alexander-University Erlangen-Nuremberg* *3. Fraunhofer Institute for Silicon Technology (ISIT)* *alexander.hensel@faps.fau.de*
2:50pm	**B-18 - ID 220 - Scratch Test Methodology for Leadframe Coating** Author(s) - Chen Ho Ong, Alfred Yeo, Hui Teng Wang *Infineon Technologies Asia Pacific, Singapore; chenho.ong@infineon.com*

Technical Session S09: Materials and Processing Chair: **Ramachandran Krishnan Trichur** Room: Lyrebird Room	
1:20pm	**Invited-04: UV Laser Releasable Temporary Bonding Materials for Advanced Packaging technologies:** Dr. Kenzo Ohkita (JSR)
1:50pm	**B-04: ID 175 - The Effects of Silica Filler Content in NCP on the Reliability of 3D TSV Multi-Stack** *Author(s) - Wagno Alves Braganca Junior[1], Yong-Sung Eom[2], Jihye Son[2], Keon-Soo Jang[2], Hyun-Cheol Bae[2], Seok Hwan Moon[2], Kwang-Seong Choi[1,2]* *1. University of Science and Technology, Korea* *2. ICT Materials and Components Laboratory, ETRI, Korea* *wagnojunior@etri.re.kr*
2:10pm	**B-09: ID 296 - Higher Reliability for Low-temperature Curable Positive-Tone Photosensitive Dielectric Materials** Author(s) - Takenori Fujiwara, Yu Shoji, Yuki Masuda, Keika Hashimoto, Yutaro Koyama, Kimio Isobe, Hitoshi Araki, Ryoji Okuda, Masao Tomikawa *Toray Industries, Inc, Japan; Takenori_Fujiwara@nts.toray.co.jp*
2:30pm	**B-14: ID 227 -** One Micron Redistribution for Fan-Out Wafer Level Packaging Author(s) - Warren W Flack[1], Robert Hsieh1, Gareth Kenyon[1], Ha-Ai Nguyen[1], John Slabbekoorn[2], Samuel Suhard[2], Andy Miller[2] *1. Ultratech, San Jose, CA, United States of America* *2. IMEC, Leuven, Belgium* *wflack@ultratech.com*
2:50pm	**B-19: ID 166 - High Reliability Low Temperature Pb-Free Alloy for Solder Hierarchy** Author(s) - Pritha Choudhury, Morgana Ribas, Siuli Sarkar *Alpha Assembly Solutions, MacDermid Performance Solutions R&D Centre, India; morgana.ribas@alphaassembly.com*

Technical Session S10: Interconnection Technologies Chair: **Evelyn Napetschnig** Room: Falcon Room	
1:20pm	**Invited-05: Trends in SIP and Placement Approaches:** Chong Chan Pin (KNS)
1:50pm	**B-05: ID 144 - Effects of Pd distribution at free air ball in Pd coated Cu wire** *Author(s) - Byung Hoon Jung[1,2], Byung Kwan Yu[1], Seung Hyun Kim[1], Jeong Tak Moon[1], Sang Jeen Hong[2]* *1. MK Electron Co. Ltd.,, Korea, Republic of (South Korea)* *2. Myongji University, Cheoin-gu Yongin, Gyeonggo-do, (South Korea)* *bhjung@mke.co.kr*
2:10pm	**B-10: ID 208 - Low Temperature Cu-Cu Bonding Using Tin Nanoparticles Fabricated by High Pressure Magnetron Sputtering** Author(s) - TZijian Wu[1], Qian Wang[1], Jian Cai[1,2] *1. Institute of Microelectronics, Tsinghua University, Beijing, 100084, China* *2. Tsinghua National Laboratory for Information Science and Technology, Tsinghua University, Beijing, 100084, China* *wu-zj12@mails.tsinghua.edu.cn*
2:30pm	**B-15: ID 224 - Bond Pad Effects on Shear Strength of Copper Wire Bonds** Author(s) - Stevan G Hunter[1], Subramani Manoharan[2], Patrick McCluskey[2] *1. ON Semiconductor, United States of America* *2. University of Maryland* *sputterman0@gmail.com*
2:50pm	**B-20: ID 237 - Leading Edge Die Stacking and Wire Bonding Technologies for Advanced 3D Memory Packages** *Author(s) - Oranna Yauw[1], Andrew Tan[1], Aashish Shah[2], Jeong Ho Yang[1], Ivy Qin[2], Jie Wu[1], Gary Schulze[2]* *1. Kulicke & Soffa Pte. Ltd.* *2. Kulicke & Soffa Industries Inc.* *wmoyauw@kns.com*

Technical Sessions C

Thursday, 7th December 2017, 4:30pm - 5:50pm

Technical Session S-11: Mechanical modeling & simulation Chair: **Santosh Kumar** Room: Paradiso Room	
4:30pm	**C-01: ID 193 - Strip Warpage Assessment of Dual Side Molding SiP Module** Author(s) - Ming-Han Wang, Ian Hu, Richard YC Chen, Chan-Lin Yeh, Meng-Kai Shih, David Tarng *Advanced Semiconductor Engineering, Inc, Taiwan; Carter_wang@aseglobal.com*
4:50pm	**C-06: ID 194 - A Comprehensive Study on BGA Block Warpage and Prediction methodology** Author(s) - Jing-en Luan *STMicroelectronics Pte Ltd, Singapore; jing-en.luan@st.com*
5:10pm	**C-11: ID 201 - Glue Selection for Robust Wire Bonding Process Related to Non-Stick on Pad** Author(s) - Ee Lin Chung[1], Dandong Ge[2], Chee Mun Wai[1] *1. Infineon Technologies (Malaysia) Sdn Bhd.* *2. Infineon Technologies Asia Pacific Pte Ltd, Singapore* *EeLin.Chung@infineon.com*
5:30pm	**C-16: ID 216 - Constitutive Model for SMA Considering Arbitrary Thermal-Mechanical Loading and Loading History** Author(s) - Xiaoyong Zhang, Dawei Huang, Mingjing Qi, Xiaojun Yan *Beihang University, People's Republic of China; zhangxy@buaa.edu.cn*

Technical Session S-12: Quality, Reliability & FA Chair: **Karsten Meier** Room: Cardinal Room	
4:30pm	**C-02: ID 163 - Risk Assessment Study of New Product Development** *Author(s) - Kazuaki Ano* *Dialog Semiconductor, Japan; kazuaki.ano@diasemi.com*
4:50pm	**C-07: ID 164 - Application of Failure Analysis on Package Copper Pillar Bump Electromigration** Author(s) - Wei-Chiao Wang, Kuan-I Cheng, Sung-Mao Wu *Micro Electrical Packaging Laboratory, Taiwan; josephgun125@gmail.com*
5:10pm	**C-12: ID 197 - Scanning Acoustic Microscopy: Resolution Reduction due to Attenuation of Acoustic Signal in Materials** Author(s) - Chiu Soon Wong *Infineon Technologies (Malaysia) Sdn. Bhd., Malaysia; chiusoon.wong@infineon.com*
5:30pm	**C-17: ID 295 - Board Level Solder Reliability Simulation for Epoxy Mold Compound Based Power Package** Author(s) - Qiuxiao Qian[1], Yong Liu[2] *1. On Semiconductor, People's Republic of China* *2. On Semiconductor, USA* *richard.qian@onsemi.com*

Technical Session S-13: Thermal Characterization & cooling solutions Chair: **Marta Rencz** Room: Swallow Room	
4:30pm	**C-03: ID 112 - Compact Heat Exchanger Design and Energy Efficiency Optimization for Data Centre Cooling Application** Author(s) - GONG YUE TANG, YONG HAN, XIAO WU ZHANG *Institute of Microelectronics, Singapore; tangg@ime.a-star.edu.sg*
4:50pm	**C-08: ID 155 - Optimal Design of a microchannel heat sink with a pin-fin array integrated with Si interposer** Author(s) - Yunna Sun, Taegyu Kang, Jian Li, Zhiyu Jin, Xinyue Chang, Yan Wang, Zhuoqing Yang, Guifu Ding *Shanghai Jiao Tong University, People's Republic of China; Cecilia_Sun@sjtu.edu.cn*
5:10pm	**C-13: ID 135 - Hybrid Micro-Fluid Heat Sink for High Power Dissipation of Liquid-Cooled Data Centre** Author(s) - Yong Han, Gongyue Tang, Boon Long Lau, Xiaowu Zhang *Institute of Microelectronics, A*STAR, Singapore; hany@ime.a-star.edu.sg*
5:30pm	**C-18: Partner Conference Introduction**

Technical Session S-14: Emerging Technologies Chair: **Cher Ming Tan** Room: Lyrebird Room	
4:30pm	**C-04: ID 213 - Oxide Surface Roughness Optimization of BiCMOS BEOL Wafers for 200 mm Wafer Level Microfluidic Packaging Based on Fusion Bonding** Author(s) - Mesut Inac[1,2], Matthias Wietstruck[2], Alexander Göritz[2], Barbaros Cetindogan[2], Canan Baristiran-Kaynak[2], Marco Lisker[2], Andreas Krüger[2], Andreas Trusch[2], Ulrike Saarow[2], Patric Heinrich[2], Thomas Voss[2], Mehmet Kaynak[2,3] *1. Technical University Berlin, Germany* *2. IHP, Frankfurt (Oder), Germany* *3. Sabanci University, Istanbul, Turkey* *inac@tu-berlin.de*
4:50pm	**C-09: ID 162 - Hybrid Hermetic Housings for Active Implantable Neural Device** Author(s) - CHENG Ming-Yuan, CHEN Weiguo, LIM Ruiqi, DAMALERIO Ramona *Institute of Microelectronics, A*STAR, Singapore; chengmy@ime.a-star.edu.sg*
5:10pm	**C-14: ID 108 - Fabrication of paper electrode by dry transfer of Ag NP and Ag NW** Author(s) - Sunho Kim, Hoo-Jeong Lee *Sungkyunkwan University, Korea, Republic of (South Korea); sunhofy@skku.edu*
5:30pm	**C-19: ID 231 - Study of Critical Load Force towards Thin Plating on PrePlated Leadframe** Author(s) - Hui Teng Wang, Chen Ho Ong, Wu Hu Li, Xiao Jun Wang, Lay Peng Ng *Infineon Technologies Asia Pacific, Singapore; huiteng.wang@infineon.com*

Technical Session S-15: Electrical Simulation & Characterization Chair: **Mihai Dragos Rotaru** Room: Falcon Room	
4:30pm	**C-05: ID 146 - Efficient Decoupling and Filtering for Multiple Loads and Voltage Domains with Composite Capacitors** Author(s) - Chin Lee Kuan[1], Amit K. Jain[2], Sameer Shekhar[2] *1. Intel Microelectronics (M) Sdn. Bhd, Malaysia* *2. Intel Corporation, Hillsboro, OR 97124, USA* *chin.lee.kuan@intel.com*
4:50pm	**C-10: ID 130 - 2.5D Silicon Optical Interposer for 400G Electronic-Photonic Integrated Circuit Platform Packaging** Author(s) - Do-Won Kim, K. Y. Au, H. Y. Li, X. S. Luo, Y. L. Ye, Surya Bhattacharya, Gou-Qiang Lo *Institute of Microelectronics, Singapore; kimd@ime.a-star.edu.sg*
5:10pm	**C-15: ID 180 - Distributed DC Electrical Assessment of Switch-Mode Convertors** Author(s) - Sameer Shekhar[1], Amit Kumar Jain[1], Chin Lee Kuan[2] *1. Intel, United States of America* *2. Intel, Malaysia* *sameer.shekhar@intel.com*
5:30pm	**C-20: ID 191 - Low transmission loss flexible substrates using low Dk/Df polyimide adhesives** Author(s) - Takashi Tasaki, Atsushi Shiotani, Takashi Yamaguchi, Keisuke Sugimoto *ARAKAWA CHEMICAL INDUSTRIES, LTD., Japan; tasaki@arakawachem.co.jp*

Technical Sessions D

Friday, 8th December 2017, 9:00am - 10:20am

Technical Session S-16: Interconnection Technologies Chair: **Chan Pin Chong** Room: Paradiso Room	
8:30am	**Invited-06: Wafer Bonding – An Enabling Technology for 3DIC, MEMS, BSI CIS, SOI, RF Filters, and More:** Eric Pabo (EVG)
9:00am	**D-01: ID 104 - Challenge and Warpage Optimization of Thermal Compression Bonding Technology on Coreless Substrates** Author(s) - Mike Tsai, Jensen Tsai, Yan Han Yao, Roger Lo, Cheng Kai Chang, Nicholas Kao *Siliconware Precision Industries Co. Ltd., Taiwan; miketsai@spil.com.tw*
9:20am	**D-06: ID 266 - Ultra-Fine-Pitch Bonding Based On Photolithography And Electroplating** Author(s) - Dongyang Li[1], Xuhan Dai[2], Taegyu Kang[3], Guifu Ding[4] *1. Department of Micro/Nano Electronics, Shanghaijiaotong University, People's Republic of China* *2. Department of Micro/Nano Electronics, Shanghaijiaotong University, People's Republic of China* *Samsung Electronics* *3. Department of Micro/Nano Electronics, Shanghaijiaotong University, People's Republic of China* *hildy7@163.com*
9:40am	**D-11: ID 305 - Digital Micro-Dispension Of Non-Conductive Adhesives (Nca) By Inkjet Printer** Author(s) - Ali Roshanghias, Alfred Binder *CTR Carinthian Tech Research AG, Austria; ali.roshanghias@ctr.at*
10:00am	**D-16: ID 281 - Novel Coated Silver (Ag) Bonding Wire: Bondability and Reliability** Author(s) - Senthilkumar Balasubramanian, Kang Il Tae, Lois Liao Jin Zhi, Evonne Evonne, Murali Sarangapani, Chee Wei Tok, James Kim Tae Yeop, Eric Tan Swee Seng, Xi Zhang *Heraeus Materials Singapore Pte Ltd, Singapore; senthilkumar.balasubramanian@heraeus.com*

Technical Session S-17: Emerging Technologies Chair: **Yan Cheong Chan** Room: Cardinal Room	
8:30am	**Invited-07: VCSEL-based Optical Interconnects and Their Packaging Technologies:** Dr. Hideyuki Nasu (Furukawa Electric Co)
9:00am	**D-02: ID 170 - Direct printing of electrical connections from metal melts using StarJet technology** Author(s) - Michael Jehle[1], Björn Gerdes[1], Pavel Soukup[2], Michael Fechtig[1], Roland Zengerle[1], Peter Koltay[1], Lutz Riegger[1] 1. *University of Freiburg, Germany* 2. *Advacam s.r.o.* *michael.jehle@imtek.uni-freiburg.de*
9:20am	**D-07: ID 288 - Ag Nanoparticles - Based Hybrid Ink with Low Metallization Temperature** Author(s) - Yongdian Han *Tianjin University, People's Republic of China; hanyongdian@tju.edu.cn*
9:40am	**D-12: ID 298 - Evaluation of Printed Capacitive Touch Sensors for Touch Panel** Author(s) - W. FAN, B. K. LOK, F. K. LAI, J. WEI *SIMTech, Singapore; wfan@SIMTech.a-star.edu.sg*
10:00am	**D-17: ID 214 - Novel End-Point Solution for Improvement in Die Strength and Yields with Plasma Dicing After Grind in Volume Production** Author(s) - Richard Barnett, Oliver Ansell, Martin Hanicenic, Janet Hopkins *SPTS Technologies Ltd, United Kingdom; richard.barnett@orbotech.com*

Technical Session S-18: Material and Processing Chair: **Rajoo Ranjan** Room: Swallow Room	
8:30am	**Invited-08: Temporary Bonding Materials for Fan-out Packaging Processes:** Ram Trichur (Brewer Science)
9:00am	**D-03: ID 230 - High Temperature Endurable Die Attach Material for Power Electronics Package – Process Challenges** *Author(s) - Leong Ching Wai, Mian Zhi Ding, GongYue Tang* *Institute of Microelectronic, Singapore; wailc@ime.a-star.edu.sg*
9:20am	**D-08: ID 292 - Development of next generation Solder Resist** Author(s) - Nobuhito Komuro, Yuta Daijima, Shinya Imabayashi *Hitachi Chemical, Japan; nobu-komuro@hitachi-chem.co.jp*
9:40am	**D-13: ID 181 - Effect of indium on the deformation properties of binary In-Bi alloys** Author(s) - Sanghun Jin[1,2], Min-Su Kim[1], Shutetsu Kanayama[3], Hiroshi Nishikawa[1] 1. *Joining and Welding Research Institute, Osaka University, Japan* 2. *Graduate School of Engineering, Osaka University, Japan* 3. *Connected Solutions Company, Panasonic Corporation, Japan* *passionista82@gmail.com*

10:00am	**D-18: ID 189 - Electromigration Polarity Effect of Cu/Ni/Sn-Ag Microbumps for Three-Dimensional Integrated Circuits** Author(s) - Hyondong Ryu, Kirak Son, Gahee Kim, Jina Lee, Young-Bae Park *School of Materials Science and Engineering, Andong National University, Korea, Republic of (South Korea); gyehd1231@gmail.com*

Technical Session S-19: Thermal Characterization & cooling solutions Chair: **Gong Yue Tang** Room: Lyrebird Room	
8:30am	**Invited-09: On-Chip Embedded Cooling of Power and Logic Components:** Dr. Avram Bar-Cohen (Raytheon Corporation)
9:00am	**D-04: ID 171 - Thermal Characterization of Dual Side Molding SiP Module** Author(s) - Tang-Yuan Chen, Bo-Syun Chen, Jin Feng Yang *Advanced Semiconductor Engineering Inc., Taiwan; Phidia_Chen@aseglobal.com*
9:20am	**D-09: ID 173 - Measurement issues in LED characterization for Delphi4LED style combined electrical-optical-thermal LED modeling** Author(s) - Marta Rencz[1,2], Gusztav Hantos[2], Janos Hegedus[2], Marton Bein[1], Lajos Gaal[1], Gabor Farkas[1], Zoltan Sarkany[1], Sandor Ress[1,2], Andras Poppe[1,2] *1. Mentor Graphics, Hungary* *2. Budapest University of Technology* *Marta_rencz@mentor.com*
9:40am	**D-14: ID 192 - Comparison of temperature distribution in FinFETs and GAAFETs based on Dual-Phase-Lag heat transfer model** Author(s) - Tomasz Raszkowski, Agnieszka Samson, Mariusz Zubert, Marcin Janicki *Lodz University of Technology, Poland; traszk@dmcs.pl*
10:00am	**D-19: ID 265 - Development of the high efficiency cooling structure of the liquid immersion cooling SR motor** Author(s) - Daiki Wakabayashi[1], Qiang YU[1], Yoshinobu Nakamura[2] *1. Yokohama National University, Japan* *2. NIDEC CORPORATION, Japan* *wakabayashi-daiki-pk@ynu.jp*

Technical Session S-20: Quality, Reliability & FA Chair: **Chai Tai Chong** Room: Falcon Room	
8:30am	**Invited-10: Reliability Assurance: A Semiconductor Supplier's Perspective:** Dr. Stevan G. Hunter (ON Semiconductor)
9:00am	**D-05: ID 198 - The influence of the cycling parameters on the reliability test results of IGBTs** Author(s) - Zoltan Sarkany[1], Marta Rencz[1,2] *1. Mentor Graphics, Hungary* *2. Budapest University of Technology and Economics* *zoltan_sarkany@mentor.com*
9:20am	**D-10: ID 243 - Measuring methods and measuring errors in electronics production technologies** Author(s) - Martin Oppermann, Thomas Zerna *Technische Universitaet Dresden, Centre for Microtechnical Manufacturing; martin.oppermann@tu-dresden.de*
9:40am	**D-15: ID 268 - GaAs Device Two-Steps Junction Stain and Scanning Capacitance Microscopy Sample Preparation** Author(s) - Yih-Sheng Chuang, Chun-An Huang, Ju-Hung Hsu, Yung-Jen Wu *Integrated Service Technology; frank_chuang@isti.com.cn*
10:00am	**D-20: ID 279 - Solder Joint Fatigue Analysis under Combined Thermal and Vibration Loading** Author(s) - Karsten Meier[1], Mike Roellig[2], Yifan Liu[1], Karlheinz Bock[1] *1. Technische Universität Dresden, Electronics Packaging Laboratory, Germany* *2. Fraunhofer Institute for Ceramic Technologies and Systems - Material Diagnostics, Germany* *karsten.meier@tu-dresden.de*

Technical Sessions E

Friday, 8th December 2017, 11:10am - 12:30am

Technical Session S-21: Materials and Processing Chair: **Kenzo Ohkita** Room: Paradiso Room	
11:10am	**E-01: ID 124 - Environmental Impact Analysis Of Mi Band 2 Smart Wristband Watch Using Simapro Tools and X-Ray Fluorescence Analyzer (XRF)Technique** Author(s) - Man Man Ma *EPA Centre,City University of Hong Kong, Hong Kong S.A.R. (China); manmanma2-c@my.cityu.edu.hk*
11:30am	**E-06: ID 153 - Photo-Dielectric Polymer Material Characterisation To Improve Reliability 3D-Ic Packaging** Author(s) - Nacima Allouti, Pascal Chausse, Stephane Moreau, Anais D'affroux *CEA, France; nacima.allouti@cea.fr*
11:50am	**E-11: ID 159 - Moisture Sensitivity Level One (1) Packaging Solution for a Nickel-Palladium-Gold (NiPdAu) Pre-plated Frames** Author(s) - Alvin Denoyo, Ariel Tan, Jun Berte, Robert Altar *ON Semiconductors, Philippines; Alvin.Denoyo@onsemi.com*
12:10pm	**E-16: ID 254 - Perfect Molding Challenges and The Limitations** Author(s) - Lay Tatt Tan, Yin Yin Teo, Chee Hong Lee, Boon Huat Lim *Infineon Technology (Malaysia), Malaysia; laytatt.tan@infineon.com*

Technical Session S-22: Advanced Packaging Chair: **Jean Charbonnier** Room: Cardinal Room	
11:10am	**E-02: ID 275 - Wafer Level Vacuum Packaging with Al-Ge bonding for MEMS** Author(s) - Daw Don Cheam, Jae-Wung Lee, Bang Tao Chen, Navab Singh *Institute of Microelectronics, Singapore; leejw@ime.a-star.edu.sg*
11:30am	**E-07: ID 116 - Development of Chip on wafer Bonding with Non-Conductive Film using Gang Bonder** Author(s) - Ser Choong Chong, Hongyu Li, Ling Xie, Sekhar Vasarla Nagendra, Daniel Ismael Cereno *Institute Of Microelectronics, Singapore; chongsc@ime.a-star.edu.sg*
11:50am	**E-12: ID 222 - Reaction competition in micro-bump and the influences on reliabilities** Author(s) - Yi-Ting Henry Chen, Raghu Chaware, Inderjit Singh, Ramasamy Anandan *Xilinx; ramasam@xilinx.com*
12:10pm	**E-17: ID: 251 - Copper nanoparticle paste on different metallic substrates for low temperature bonded interconnection** Author(s) - Jaewon Kim[1], Byunghoon Lee[2], Ja-Myeong Koo[2], Chee Lip Gan[1] *1. Nanyang Technological University, Singapore* *2. Global technology center, Samsung Electronics, Yeongtong-Gu, Suwon-si, Korea* *jwkim@ntu.edu.sg*

Technical Session S-23: TSV/Wafer Level Packaging Chair: **Boo Yang Jung** Room: Swallow Room	
11:10am	**E-03: ID 247 - Development of Chip-First and Die-Up Fan-out Wafer Level Packaging** Author(s) - Li Zhang[1], Dong Chen[1], Hong Xu[1], Xuan Hua[1], KH Tan[1], CM Lai[1], John Lau[2], Ming Li[2], Margie Li[2], Eric Kuah[2], Nelson Fan[2], Kai Wu[2], Ken Cheung[2] *1. Jiangyin Changdian Advanced Packaging Co.,LTD* *2. ASM Pacific Technology* *Tony_Chen@jcap.com.cn*
11:30am	**E-08: ID 195 - Through-Silicon Via Process Module with Backside Metallization and Redistribution Layer within a 130 nm SiGe BiCMOS Technology** Author(s) - Matthias Wietstruck[1], Steffen Marschmeyer[1], Marco Lisker[1], Andreas Krueger[1], Dirk Wolansky[1], Mirko Fraschke[1], Philipp Kulse[1], Alexander Goeritz[1], Mesut Inac[1,2], Thomas Voss[1], Andreas Mai[1], Mehmet Kaynak[1,3] *1. IHP Microelectronics, Germany;* *2. Technical University Berlin, Germany* *3. Sabanci University, Turkey* *wietstruck@ihp-microelectronics.com*
11:50am	**E-13: ID 218 - Plating Challenges Associated with High-Density Fan-Out (HDFO) Technology** Author(s) - Kari Thorkelsson *Lam Research Corporation, United States of America; kari.thorkelsson@lamresearch.com*
12:10pm	**E-18: ID 103 - Integration Benefits and Challenges on Fan-Out to Enable System in Package for IoT/Wearable Devices** Author(s) - Humi Tang[1], Max Lu[2], Jensen Tsai[3] *1. Siliconware Precision Industries Co., Ltd. (SPIL), Taiwan* *2. Siliconware Precision Industries Co., Ltd. (SPIL), Taiwan* *3. Siliconware Precision Industries Co., Ltd. (SPIL), Taiwan* *humitang@spil.com.tw*

Technical Session S-24: Electrical Simulations & Characterization Chair: **Eldon Staggs** Room: Lyrebird Room	
11:10am	**E-04: ID 186 - Establish Electrostatic Discharge Simulation Environment Combined with Near-Field measurement** Author(s) - Chia-Hsuan Tsai, Cheng-Dao Li, Sung-Mao Wu *Micro Electrical Packaging Laboratory, Taiwan; st910414@gmail.com*
11:30am	**E-09: ID 196 - Dielectric Constant Measurement using Near-Field System** Author(s) - Li-Xuan Tsai, Kuan-I Cheng, Sung-Mao Wu *Micro Electronic Packaging Laboratory, Taiwan; soply0825@gmail.com*
11:50am	**E-14: ID 211 - SMA Connector to Co-Planer Calibration** Author(s) - Chun-Ting Lai *Micro Electronic Packaging Laboratory, Taiwan* *locker010313@gmail.com*
12:10pm	**E-19: ID 228 - Automation of ATE Test Program Execution in Offline and Online** Author(s) - Deva Ruban Maria, Kamalakannan Viswanathan, Michael Baclay Amal, Karthik Krishna Kumar *Xilinx Asia Pacific Pte. Ltd., Singapore* *kvi@xilinx.com*

Technical Session S-25: Mechanical Modeling & Simulations Chair: **Yong Han** Room: Falcon Room	
11:10am	**E-05: ID 236 - Study on warpage and stress of TSV wafer with ultra-fine pitch vias for high density chip stacking** Author(s) - Faxing Che, Ling Xie, Zhaohui Chen, Sunil Wickramanayaka *IME, A-star, Singapore; chenz@ime.a-star.edu.sg*
11:30am	**E-10: ID 252 - Modeling of manufacturing induced residual stresses of viscoelastic epoxy mold compound encapsulations** Author(s) - Mario Gschwandl[1], Peter Filipp Fuchs[1], Thomas Antretter[2], Mahesh Yalagach[1], Ivaylo Mitev[1], Tao Qi[4], Angelika Schingale[3] *1. Polymer Competence Center Leoben GmbH, Austria* *2. Institute of Mechanics, University of Leoben, Austria* *3. Continental Corporation* *4. AT&S* *mario.gschwandl@pccl.at*
11:50am	**E-15: ID 125 - Trend Plots for Compound Selection Utilized for Warpage Design of MUF FCCSP with 4L ETS** Author(s) - Chih-Sung Chen, Nicholas Kao, Don Son Jiang *Siliconware Precision Industries Co. Ltd. (SPIL), Taiwan; chihsungchen@spil.com.tw*
12:10pm	**E-20: ID 278 - Thermo-Mechanical Reliability Prediction for Copper Pillar 3D IC Devices** Author(s) - Ganesh Hariharan, Raghunandan Chaware, Inderjit Singh, Anandan Ramasamy *Xilinx, United States of America; inderji@xilinx.com*

Technical Sessions G

Friday, 8th December 2017, 2:00pm - 3:20pm

Technical Session S-26: Advanced Packaging Chair: **Albert Lan** Room: Paradiso Room	
1:30pm	**Invited-11: Advanced eWLB FOWLP: Enabling Integrated Packaging Solutions:** Dr. Seung Wook Yoon (STATS ChipPAC)
2:00pm	**G-01: ID 151 - Development of Highly efficient push-pull Power Amplifier with Center Tapped Transformer for 5GHz application** *Author(s)* - Tomoki Sadakiyo, Haruichi Kanaya *Kyushu University, Japan; 2IE16616G@s.kyushu-u.ac.jp*
2:20pm	**G-06: ID 209 -Gallium Nitride transistor on glass using epoxy mediated substrate transfer technology** Author(s) - Pavani Vamsi Krishna Nittala, Nayana Ramesh, Nagaboopathy Mohan, Rangarajan Muralidharan, Srinivasan Raghavan, Digbijoy N Nath, Prosenjit Sen *CeNSE, Indian Institute of Science, Bangalore; vamsinittala@gmail.com*
2:40pm	**G-11: ID 179 - Challenges of Ultra Thin WLCSP** Author(s) - Kelly Chen[1], Tom Tang[1], Mark Liao[1], Jensen Tsai[1], Steve Hsieh[2], Jerry Chang[2], Arthur Ho[2] *1. SPIL, Taiwan* *2. NXP, Taiwan* *kellychen@spil.com.tw*
3:00pm	**G-16: ID 174 - Wafer-Level Packaging Technology for Optical Sensor Devices** Author(s) - Gregor Toschkoff, Thomas Bodner, Harald Etschmaier, Franz Schrank *ams AG, Austria; gregor.toschkoff@ams.com*

Technical Session S-27: TSV/Wafer Level Packaging Chair: **Inderjit Singh** Room: Cardinal Room	
1:30pm	**Invited-12: Highly accurate TSV, PWB and FO-PLP wiring fabication by plasma dry processes for interface:** Dr. Yasuhiro Morikawa (ULVAC)
2:00pm	**G-02: ID 304 - Enabling faster design and implementation decisions using virtual prototyping** *Author(s)* - Yoko Fujita *ZUKEN Inc., Japan; fujita.yoko@zuken.co.jp*
2:20pm	**G-07: ID 177 - Impact of 3D Stacking on the TSV-induced Stress and the CMOS Characteristics** Author(s) - Aki Dote, Hiroko Tashiro, Hideki Kitada, Shinji Tadaki, Shoichi Miyahara, Seiki Sakuyama *Fujitsu Ltd., Japan; dote.aki@jp.fujitsu.com*
2:40pm	**G-12: ID 250 - Effective Layout Scheme of Power and Ground TSVs for More Reliable Power Delivery in 3-D ICs** Author(s) - Weijun Zhu, Gang Dong, Zheng Mei *Xidian University, People's Republic of China; mmzzkkxx@126.com*
3:00pm	**G-17: ID 221 - Dispensing Challenges of Large Format Packaging and Some of Its Possible Solutions** Author(s) - Eric Teng Hock Kuah, Wei Ling Chan, Ji Yuan Hao, Chun Ho Fan, Ming Li, John Lau, Kai Wu *ASM Technology Singapore Pte Ltd, Singapore; eric.kuah@asmpt.com*

Technical Session S-28: Interconnection Technologies Chair: **Guilian Gao** Room: Swallow Room	
1:30pm	**Invited-13: 10 Golden Rules of Chip- Package- Board Interactions:** Dr. E.Napetschnig (Infineon Technologies Austria)
2:00pm	**G-03: ID 120 - Challenges of Wirebonding with Polyimide Flexible Circuit Board(FPCB)** Author(s) - Norhanani Jaafar, Ramona Damalerio *Institute of Microelectronic, Singapore; jaafarn@ime.a-star.edu.sg*
2:20pm	**G-08: ID 105 - More than Moore and Beyond CMOS: New Interconnects Schemes and New Circuits Architectures** Author(s) - Khaled Salah Mohamed *Mentor, Egypt; khaled_mohamed@mentor.com*
2:40pm	**G-13: ID 217 - Challenges and feasibility of Ag wire bonding for Automotive Applications** Author(s) - Jing-en Luan *STMicroelectronics Pte Ltd, Singapore; jing-en.luan@st.com*
3:00pm	**G-18: ID 114 - Optimizing Ag Wire Bonding for Memory Devices** Author(s) - Ivy Qin[1], Gary Schulze[1], Tom Rockey[1], Basil Milton[1], Bob Chylak[1], Nelson Wong[2] *1. kulicke and soffa industries inc., United States of America* *2. kulicke and soffa Pte Ltd, Singapre* *iqin@kns.com*

Technical Session S-29: Emerging Technologies Chair: **Jun Su Lee** Room: Lyrebird Room	
1:30pm	**Invited-14: Heterogeneous Integration Roadmap - Global Collaboration:** William Chen, ASE Group
2:00pm	**G-04: ID 249 - Additive low temperature 3D printed electronic as enabling technology for IoT application** Author(s) - Serguei Stoukatch[1], Francois Dupont[1], Laurent Seronveaux[2], Denis Vandormael[2], Michael Kraft[1] *1. University of Liege, Belgium* *2. Sirris, Belgium* *Serguei.stoukatch@ulg.ac.be*
2:20pm	**G-09: ID 244 - Stress-Free Bonding Technology with Bondable Thin Glass layer for MEMS based Pressure Sensor** Author(s) - Ha-Duong Ngo[1,3], Xiaodong Hu[2,4], Oswin Ehrmann[2,3], Klaus-Dieter Lang[2,3], Martin Schneider-Ramelow[2,3], Ulli Hansen[4] *1. University of Applied Sciences, Germany* *2. Technical University Berlin* *3. Fraunhofer Institut IZM* *4. MSG Lithoglas GmbH* *hu@mat.ee.tu-berlin.de*
2:40pm	**G-14: ID 161 - Design of NFC WISP system for wearable devices** Author(s) - Xuesong Zhang, Qian Wang, Han Guo, Yu Chen, Jian Cai *Tsinghua University, People's Republic of China; zhangxs15@mails.tsinghua.edu.cn*
3:00pm	**G-19: ID 253 - Growth and Fabrication of Carbon-Based Three-Dimensional Heterostructure in Through-Silicon Vias (TSVs) for 3D Interconnects** Author(s) - Ye Zhu, Chong Wei Tan, Shen Lin Chua, Yu Dian Lim, Beng Kang Tay, Chuan Seng Tan *Nanyang Technological University, Singapore; yzhu012@e.ntu.edu.sg*

Technical Session S-30: Electrical Simulations & Characterization Chair: **Ranauld Perez** Room: Falcon Room	
1:30pm	**Invited-15: Reliability of Electronic Packages:** Prof. Tan Cher Ming (Chang Gung University, Taiwan)
2:00pm	**G-05: ID: 257 - Inductance Characterization and Improvement on a Small GQFN Package** Author(s) - Carolyn Tubillo, Kyaw Ko Lwin, Jun Dimaano, Dr. Nathapong Suthiwongsunthorn *UTAC Headquarters Pte. Ltd, Singapore; kolwin_kyaw@utacgroup.com*
2:20pm	**G-10: ID 245 - FOWLP Design for HBM Applications** Author(s) - Teck Guan LIM *A*STAR IME, Singapore; limtg@ime.a-star.edu.sg*
2:40pm	**G-15: ID 270 - Investigating the Role of Sidewall Surface Roughness on the Performance of Through Silicon Vias** Author(s) - Rohit Y Sharma, Somesh Kumar, Sunil Pathani *Indian Institute of Technology Ropar, India; Somesh.Kumar@iitrpr.ac.in*
3:00pm	**G-20: ID 233 - Analysis and design of low loss transmission line structure for high speed applications** Author(s) - Mihai Dragos Rotaru *University of Southampton, Malaysia; mdr1f06@soton.ac.uk*

Interactive Presentations

Interactive Sessions

7th and 8th December 2017

Interactive Session #1: 7th December 2017, 10:00am - 10:30am Venue: Foyer of Grand Ballroom II, Level 4	
P01	**ID: 285 - Hybrid flexible smart temperature tag with NFC technology for smart packaging** Author(s) - Xi Zhang, Xuechuan Shan *Singapore Institute of Manufacturing Technology, Singapore* *zhangxi@Simtech.a-star.edu.sg*
P02	**ID: 241 - Process Development of Moldable Underfill on Fine Pitch RDL 1st Fan-out Wafer Level Package** Author(s) - Simon Siak Boon Lim, Mian Zhi Ding, Ser Choong Chong *Institute of Microelectronics, Singapore* *limsb@ime.a-star.edu.sg*
P03	**ID: 138 - Chip-to-Wafer (C2W) flip chip bonding for 2.5D High density interconnection on TSV free interposer** Author(s) - Pei Siang Lim, Mian Zhi Ding, Masaya Kawano *Institute of Microelectronics, Singapore* *limps@ime.a-star.edu.sg*
P04	**ID: 276 - Mechanical And Electrical Characteristics Of Screen Printed Stretchable Circuits On Thermoplastic Polyurethane** Author(s) - JSihan Joseph Chen[1], Xuechuan Shan[1], Reuben Tang[2], Vasudiva Sunappan[1], Zhaowei Zhong[2], Jun Wei[1] 1. *Singapore Institute of Manufacturing Technology* 2. *MAE, Nanyang Technological University* *shchen@SIMTech.a-star.edu.sg*
P05	**ID: 150 - Development of the Endoscopic Clip with a Battery-Less LED for Laparoscopic Gastrointestinal Resection** Author(s) - Kyohei Shibata[1], Yuharu Shinki[1], Ryosuke Tsutsumi[2], Tetsuo Ikeda[2], Haruichi Kanaya[1] 1. *Kyushu University, Japan* 2. *Kyushu University Hospital, Japan* *2ie16656p@s.kyushu-u.ac.jp*
P06	**ID: 225 - Evaluation of Thin Film Encapsulation strength for commercial packaging** Author(s) - JJae-Wung Lee, Srinivas Merugu, Ser Choong Chong, Navab Singh *Institute of Microelectronics, Singapore* *leejw@ime.a-star.edu.sg*
P07	**ID: 182 - Design and Electrical Analysis for Advanced Fan-out Package-on-Package** Author(s) - Pan Po-Chih, Hsieh Tsun-Lung, Huang Chih-Yi, Jhong Ming-Fong, Wang Chen-Chao *Advanced Semiconductor Engineering Group, Taiwan* *Powei_Pan@aseglobal.com*

P08	**ID: 226 - Thermal Design and Analysis of Through Silicon Interposer (TSI) Package** Author(s) - LIN BU *IME, Singapore* *bul@ime.a-star.edu.sg*
P09	**ID: 284 - Nanomechanical Properties of Pressure-Less Sintered Silver Nanoparticles** Author(s) - Xu Long[1], Wenbin Tang[1], Weijuan Xia[2] *1. Northwestern Polytechnical University, People's Republic of China* *2. Space Research Institute of Electronics and Information Technology, Aerospace Science and Technology Corporation* *xulong@nwpu.edu.cn*
P10	**ID: 242 - Evaluation of Single Layer Adhesive Material for Thin Wafer Handling Applications** Author(s) - Nagendra Sekhar Vasarla[1], Hongmiao JI[1], Shinji ARIMOTO[2], Toru OKAZAWA[2], Takenori FUJIWARA[2], Masaya KAWANO[1] *1. Institute of Microelectronics, Singapore* *2. Toray Industries, Inc., Japan* *vasarla@ime.a-star.edu.sg*
P11	**ID: 215 - Wideband Modeling and Characterization of Coaxial-annular through-silicon via for 3-D ICs** Author(s) - Zheng Mei, Gang Dong *Xidian University, People's Republic of China* *mmzzkkxx@126.com*
P12	**ID: 133 - Modelling Of Wire Bonding Cu-Al Intermetallic Formation Growth Towards Interfacial Stress** Author(s) - Cher Chia LEE[1], Kok Yau CHUA[1], Anand T. Joseph Sahaya[2], Shariza Sharir[2], Mohamad Ridzuan Jamli[2] *1. Infineon Technologies (Advanced Logic) Sdn Bhd, Malaysia* *2. Faculty of Manufacturing Engineering, University Technical Malaysia Melaka* *cherchia.lee@infineon.com*
P13	**ID 126 - A Novel Annular Ring Design for Improved Plated-Through-Hole Impedance Matching** Author(s) - Jackson Kong[1], Bok Eng Cheah[1], Khang Choong Yong[1], Howard Heck[2] *1. Intel Microelectronics (M) Sdn. Bhd.* *2. Intel Corporation* *jackson.kong@intel.com*
P14	**ID 204 - Passive Stress Sensor Development: From 65nm to 28nm Technology Nodes** Author(s) - Idir Raid[1], Rafael Estevez[2], Sébastien Gallois-Garreignot[1], Olivier Kermarrec[1] *1. STMicroelectronics, 850 rue Jean Monnet, 38926 Crolles Cedex, France* *2. SIMaP, Grenoble INP, CNRS UMR5266, 1130 rue de la Piscine, BP 75 38402 Saint Martin D'Hères, France* *idir.raid@st.com*

Interactive Session #2: 8th December 2017, 3:20pm - 3:50pm Venue: Foyer of Grand Ballroom II, Level 4	
P01	**ID: 238 - Study of underfill dispensing for a large-die package** Author(s) - Huei Nuan Huang, Matt Tseng, Chung Liang Liu, Cheng Sheng Xu, Kun Hung Lin, Che Min Chu, Yu Huci Tsai *SPIL, Taiwan* *hnhuang@spil.com.tw*
P02	**ID: 229 - Characterization of Molding Compound Material and Dielectric of RDL Layers** Author(s) - Zihao Chen, Teck Guan Lim *IME, A*STAR, Singapore* *chenzh@ime.a-star.edu.sg*
P03	**ID: 219 - Factors affecting activation energy for Pd-coated Cu ball bond resistance degradation on Al bond pads in high temperature storage** Author(s) - Stevan G Hunter[1], Michael D Hook[2], Michael Mayer[2] *1. ON Semiconductor, United States of America* *2. University of Waterloo* *sputterman0@gmail.com*
P04	**ID: 302 - Study on the Impact of Primer Process Control and Lead Delamination Towards Cracked/ Broken Wedge Bond** Author(s) - Shu Hui Goh, Chee Kiang Lau, Kim Seng Chang *Infineon Technology, Malaysia* *SHUHUI.GOH@INFINEON.COM*
P05	**ID: 129 - Package with Simulation Method To Predict Underfill Flow Pattern with Different Dispensed Condition** Author(s) - ChiaHung Yen, Hung Leo, Nicholas Kao, Don Son Jiang *SPIL, Taiwan* *freedman@spil.com.tw*
P06	**ID: 255 - The fabrication of transmission line on the glass substrate** Author(s) - Hongyu Li, Do-Won Kim, Sekhar Vasarla *IME, Singapore* *lihy@ime.a-star.edu.sg*
P07	**ID: 289 - The mechanism and damage of snail trails** Author(s) - Shudong Zhou *Guangzhou bothleader electrical material co.ltd., China* *gzbld@hotmail.com*
P08	**ID: 156 - Qualitative & Quantitative Study of Flux-clean Solution for Smart High-Side Device** Author(s) - Ghizelle Abarro, Ariel Tan *ON Semiconductor Philippines Inc., Philippines* *Ghizelle.Abarro@onsemi.com*

P09	**ID: 147 - Research on Dual-Linear Motor Synchronous Control in the High-precision Gantry Motion Stage** Author(s) - Yunbo He, Wentao Ye *Guangdong University of Technology, People's Republic of China* *yewt15622352286@126.com*
P10	**ID: 136 - 2.5D Chip TSV Open Failure Analysis by High Resolution Time-domain Reflectometry** Author(s) - Masaichi Hashimoto[1], Makoto Shinohara[1], Yang Shang[1], Aparna Mohan[2], Bernice Zee[2] *1. Advantest Corporation* *2. Advanced Micro Devices* *yang.shang@advantest.com*
P11	**ID: 106 - Survey on 3D-ICs Thermal Modeling, Analysis, and Management Techniques** Author(s) - Khaled Salah Mohamed *Mentor, Egypt* *khaled_mohamed@mentor.com*
P12	**ID: 240 - Predictive Analytics in Reverse Supply Chain Management - Commodity Life Expectancy for Quality Engineering** Author(s) - Ai Kiar Ang, Alfred Degbotse, Julian SK Tan, Ngoc Vuong Quy *IBM, Singapore* *angak@sg.ibm.com*
P13	**ID: 234 - Development of Back-end Process Integration for Implantable Neurostimulation Application** Author(s) - PO-CHUN CHEN, Heng-An Ku, Pin-Cheng Lin *National Taipei University of Technology, Taiwan* *cpc@mail.ntut.edu.tw*
P14	**ID 272 - Heterogeneous interposer based integration of chips onto interposer to achieve high speed interfaces for ADC application** Author(s) - Andy Heinig, Michael Dittrich, Fabian Hopsch *Fraunhofer IIS/EAS, Germany* *andy.heinig@eas.iis.fraunhofer.de*