EPTC 2018

20th Electronics Packaging Technology Conference
4th – 7th Dec 2018, Resorts World Sentosa, Singapore

IEEE EPS Flagship Conference
In Asia Pacific Region

FINAL CALL FOR PAPERS

ABOUT EPTC

The 20th Electronics Packaging Technology Conference (EPTC 2018) is an International event organized by the IEEE RS/EPS /EDS Singapore Chapter and co-sponsored by IEEE Electronics Packaging Society (EPS). EPTC 2018 will feature keynotes, technical sessions, short courses, forums, an exhibition, social and networking activities. It aims to provide a good coverage of technology developments in all areas of electronics packaging from design to manufacturing and operation. It is a major forum for the exchange of knowledge and provides opportunities to network and meet leading experts. Since its inauguration in 1997, EPTC has developed into a highly reputed electronics packaging conference in the Asia-Pacific and is well attended by experts in all aspects of packaging technology from all over the world. EPTC is the flagship conference of IEEE EPS in Region 10. **This year, to commemorate the 20th anniversary of EPTC, one extra day of special technical presentations will be added to the conference program.**

CONFERENCE TOPICS

You are invited to submit an abstract, presenting new developments in the following categories:

- **Advanced Packaging:** Advanced Flip-chip, 2.5D & 3D, PoP, embedded passives & actives on substrates, System in Packaging, embedded chip packaging technologies, Panel level packaging, RF, Microwave & Millimeter-wave, Power and Rugged Electronics Packaging etc.
- **TSV/Wafer Level Packaging:** Wafer level packaging (Fan in/Fan out), embedded chip packaging, 2.5D/3D integration, TSV, Silicon & Glass interposer, RDL, bumping technologies, etc.
- **Interconnection Technologies:** Au/Ag/Cu/Al Wire-bond / Wedge bond technology, Flip-chip & Cu pillar, solder alternatives (ICP, ACP, ACF, NCP, ICA), Cu to Cu, Wafer level bonding & die attachment (Pb-free) etc.
- **Emerging Technologies:** Packaging technologies for MEMS, biomedical, optoelectronics, Internet of things, photo voltaic, printed electronics, wearable electronics, Photonics, LED, etc.
- **Materials and Processing:** advanced materials such 3D materials, photoresist, polymer dielectrics, solder materials, die attach, underfill, Substrates, Lead-frames, PCB etc for advanced packaging, and assembly processes using advanced materials
- **Equipment and Process Development & Automation:** processes development, equipment automation, process and equipment hardware improvements, data analytics, in-situ metrology.
- **Electrical Simulation & Characterization:** Power plane modeling, signal integrity analysis by simulations and characterization. 2D/2.5D/3D package level high-speed signal design, characterization and test methodologies.
- **Mechanical Simulation & Characterization:** Thermo-mechanical, moisture, fracture, fatigue, vibration, Shock and drop impact modeling, chip-package interaction, etc.
- **Thermal Characterization & Cooling Solutions:** Thermal modeling and simulation, component, system and product level thermal management and characterization
- **Quality, Reliability & Failure Analysis:** Component, board, system and product level reliability assessment, Interfacial adhesion, accelerated testing, failure characterization, etc.

Others are also welcomed, e.g. Market trends, Environmental, legislation, Patents, Education, Cost Analysis

IMPORTANT DATES

Online abstract submission start	30th Mar 2018
Closing of abstract submission	Extended to 27th July 2018
Notification of acceptance	15th August 2018
Submission of manuscript	15th September 2018

ABSTRACT AND PAPER SUBMISSION

Abstracts are solicited which describe original and unpublished work. The abstract should be at least 500-750 words long and clearly state the purpose, methodology, results (including data, drawings, graphs and photographs) and conclusion of the work. Key references to prior publications should be included in the abstract as well. Authors can choose between oral or interactive presentation. Accepted papers that are registered and presented (oral & interactive) at the conference will qualify for publication in IEEE Xplore.

All submissions must be in English and should be made via the online submission system found at http://www.eptc-ieee.net. The required file format is Adobe Acrobat® PDF or MS Word in one single file for each submission.

The abstracts must be received by 27th July 2018. Authors must include their affiliation, mailing address, telephone number and email address. Authors will be notified of paper acceptance and publication instruction by 15th August 2018. The final manuscript for publication in the conference proceedings is due by 15th September 2018. The conference proceedings is an official IEEE publication and accepted papers will be available in IEEE Xplore.

BEST PAPER AWARDS

Awards will be given to the best oral papers from Academia, Industry and Students, and to the best interactive papers from Student and Open categories. More details can be found at http://www.eptc-ieee.net

CALL FOR SHORT COURSES

The conference program includes short courses which will be conducted by leading experts in the field. Details will be updated in the conference website. Proposals for short courses can be submitted to pdc@eptc-ieee.net

CALL FOR EXHIBITION / SPONSORSHIP PARTICIPATION

A tabletop exhibition featuring suppliers of materials, equipment and services to the microelectronics packaging and assembly industries, will be held during the conference. For details, please e-mail to exhibition@eptc-ieee.net and sponsorship@eptc-ieee.net.

EPTC 2018: website: http://www.eptc-ieee.net Email: secretariat@eptc-ieee.net Join us on: Linkedin [EPTC OC]

Organized by
IEEE Reliability/EPS/ED Singapore Chapter

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IEEE ELECTRONICS PACKAGING SOCIETY

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PROGRAM HIGHLIGHTS

(SUBJECT TO CHANGE)

PROFESSIONAL DEVELOPMENT COURSES

- Introduction to fan-out wafer-level packaging, Dr. Beth Keser – Intel Corporation.
- Understanding flip chip technology and its applications, Dr. Eric Perfecto – Globalfoundries.
- Advanced integrated circuit design for reliability, Dr. Richard Rao – Microsemi Corp, USA.
- Introduction to 3D interconnect and packaging technologies, Prof. Sarah Kim – Seoul National University of Science and Technology.
- And more

SPECIAL 20TH ANNIVERSARY PROGRAM

Keynotes and Invited Presentations by experts:

- Ivor Barber, VP, AMD, USA.
- David McCann, VP, Globalfoundries, USA.
- Dr Avram Bar Cohen, Raytheon Corporation, USA.
- Dr. Stevan G Hunter, On Semiconductor, USA.
- Dr. Bill Chen, Fellow, ASE Group, USA.
- Prof. Robert Kao, National Taiwan University.
- Prof. Jeffrey Suhling, Auburn University, USA.
- Dr. Evelyn Napetschnig, Infineon Technologies.
- Mr. Sam Karikalan, Broadcom Inc., USA.
- Mr. Paul Werbaneth, Intevac.
- And many more

VIBRANT VENUE – RESORTS WORLD SENTOSA

World-class venue with attractions including Universal Studios, RWS Casino and theme parks.

BOG MEETING

First time ever IEEE EPS Board Of Governors meeting held outside USA. Many packaging experts who are members of BoG will be participating in the conference program.

CONFERENCE BANQUET IN S.E.A. AQUARIUM

Fine dining at a stunning and memorable backdrop with marine animals sighted through a panoramic window to the ocean.

PARTIAL LIST OF ABSTRACTS RECEIVED TO DATE

1. Guided Interconnect – The Next-Generation Flex Circuits for High-Performance System Design, J. Kong et al, Intel Corporation.
2. Study of the die position accuracy in the fabrication process of a die first type FO-PLP, K. Nishido et al, Hitachi Chemical Co. Ltd., Japan.
3. Novel concept of an in-situ test system for the thermal-mechanical reliability evaluation of electronic joints. R. Metasch et al, Fraunhofer Institute, Germany.
4. High Frequency Power Integrity Design Sensitivity to Package Design Rules, S. Shekhar et al, Intel Corporation.
5. Within-die coplanarity improvement strategies for electro-plated Cu pillars, G. Graham et al, Lam Research, USA.
6. One Micron Damascene Redistribution for Fan-Out Wafer Level Packaging using a Photosensitive Dielectric Material, R Hsieh et al, Veeco, IMEC & JSR MICRO NV, Belgium.
7. Develop Smart Wire Bonding Processes for Smart Factories, I. Qin et al, Kulicke & Soffa Inc, USA.
8. Critical Factors impacting strength of UBM in smaller and denser bumps and methodologies for optimization, A Ramasamy et al, Xilinx Singapore, USA, Taiwan.
9. Innovative Packaging Solutions of 3D System in Package with Antenna Integration for IoT and 5G Application, M. Tsai, SPIL, Taiwan.
10. Effective Electromagnetic shielding method for A new fan-out package utilizing Cu Substrate, S. Kim et al, Hanyang University, South Korea.
11. Impact of lifetime and mechanical behaviors on TIM per-formance on high-end processor, R. Gamal et al, Xilinx USA.
12. Design and optimization of the 10Tbps optical transmission system, H. He et al, Institute of Microelectronics of Chinese Academy of Sciences, China.
13. Analysis of Low Profile Ferrite Material Based Planar Shell Core Inductor, Z. Zeeshan et al, Infineon, Germany.
14. A New Failure Mechanism of Inter Layer Dielectric Crack, H. Liu et al, NXP, China.
15. Thermal Performance Characterization and Enhancement for High Power Package Development, B. S. Chen et al, Advanced Semiconductor Engineering, Inc, Taiwan.
16. Temporary Bonding Material Study for Room Temperature Mechanical Debonding with eWLB Wafer Application, S. Masuda et al, FUJIFILM Corporation, Japan.
17. Ceramic Interposers for Ultra-High Density Packaging and 3D Circuit Integration, A Adibi et al, École de Technologie Supérieure, Canada.
18. High bonding strength of silver sintered joints on non-precious metal surfaces by pressure sintering under air atmosphere using micro-silver sinter paste"; L. M. Chew et al, Heraeus Deutschland GmbH & Co. KG, Germany.
19. Design Optimization of Through-Silicon Vias for Substrate-Integrated Waveguides embedded in High-Resistive Silicon Interposer, M Wietstruck et al, IHP, Germany and Sabanci University, Turkey.
20. Millimeter-Wave Antenna in Package (AiP) Using Unbalanced Substrate with and without Solder Mask, K. T. Chen et al, SPIL, Taiwan.
21. Highly Stretchable, Durable, and Printable Textile Conductor, W. J. Lee et al, Seoul National University of Science and Technology, South Korea.

22. Failure Analysis on Mobile Phone Batteries and Accessories, Z Jin, Osaka University, Japan, City University of Hong Kong.
23. Investigations of Silver Sintered Interconnections on 3-Dimensional Ceramics with Plasma Based Additive Copper Metallizations, A. Hensel et al, Friedrich-Alexander University, Erlangen,-Nürnberg, Germany.
24. Characterization of interfacial intermetallic compounds in gold wire bonding with copper pad, B. Wang et al, Huawei.
25. Investigation on solder void formation mechanism after high temperatures stress by 3D CT scan and EDX analysis, C. Y. Lai et al, Infineon, Malaysia.
26. Via Interconnections for Half-Inch Sized Package Fabricated by Minimal Fab, National Institute of Advanced Industrial Science and Technology (AIST), Japan.
27. High Density Bumpless Interconnections Using Novel Wafer Bonding Approach For 3D IC Heterogeneous Integration Applications, K. Hemanth et al, IIT Hyderabad, India.
28. "3rd Level" Solder Joint Reliability Investigations for Transfer of Consumer Electronics in Automotive Use, R. Dudek et al, Fraunhofer ENAS, Germany.
29. Post processing of a SiN-based photonic stack above a CMOS imager sensor, N Pham et al, IMEC, Belgium.
30. Simulation And Electrical Characterization Of A Novel 2D-Printed Incontinence Sensor With Conductive Polymer PEDOT:PSS For Medical Applications, M. Baeuscher et al, Fraunhofer Institute for Reliability and Microintegration Berlin, Germany.
31. Challenges and Approaches of 2.5D high density Flip chip interconnect on through mold interposer, S. Lim et al, Institute of Microelectronics, Singapore.
32. Development of SiC Chip Based Power Package for High Power and High Performance Application, G.Y. Tang et al, Institute of Microelectronic, Singapore.
33. Laser Separation of Dissimilar Substrates Using Water Washable Materials , J Moore et al, Daetec LLC, USA.
34. Solder Mask Crack Investigation and Optimization for Larger FCBGA Package, V Lin et al, SPIL, Taiwan.
35. Wideband slot array antenna for 1 THz band imaging device, K Tsugami et al, Kyushu University, Japan.
36. Hybrid Cu-SiN and Cu-SiOx Direct Bonding of 200 MM CMOS Wafers With Five Metal Levels: Morphological, Electrical and Reliability Characterization, C Cavaco et al, IMEC, Belgium.
37. Pluggable Silicon Photonics MEMS Switch Package for Data Centre, H.Y. Hwang,Tyndall National Institute, Ireland.
38. Simulation Approach to Predict Warpage based on Resin Curing Behavior during Substrate Manufacturing Process, M Furuyama et al, Fujitsu Laboratories Ltd, Japan.
39. Si-based Hybrid Microfluidic Cooling for Server Processor of Data Centre Y. Han, Institute of Microelectronics, A*STAR, Singapore.
40. Low Transmission Loss Polyimides Substrates: A Novel Alternative to Liquid crystal polymers, T. Tasaki, Arakwa Chemical Industries Ltd., Japan.