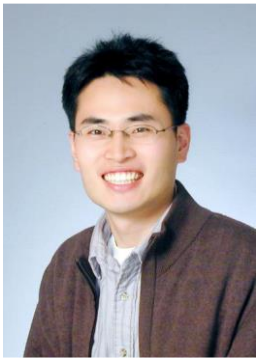
Emerging NAND Memory Packaging Challenges

Dr. Gokul Kumar is a Principal Engineer with the Packaging & Assembly Group at Western Digital, Milpitas, USA. He has a multi-disciplinary expertise in the areas of packaging of electronic systems, signal and power integrity, 3-D integration. Previously, he worked on developing 3-D interposers within the glass/silicon interposer consortia at the 3-D packaging research center in Georgia Tech. He has coauthored about 15 conference and journal publications, with 1 issue patent and 5 others pending. He regularly reviews papers for IEEE CPMT, and several other conferences including EPEPS, International Midwest Symposium on Circuits and Systems, etc.
He received his PhD and MS specializing in Electrical and Computer Engineering, from the Georgia Institute of Technology in 2015 and 2010 respectively.



Interface Pattern Void Analysis in Face to Face Hybrid Wafer Bonding

Soon-Wook Kim is senior process integration engineer at IMEC. He presently performs R&D in the field of hybrid wafer bonding focused on 3D System-On-Chip (SOC) integration for 5 years. Before joining IMEC, he took on the role of 2.5D integration project in Institute of Microelectronics (IME, Singapore). He started the semiconductor various activities at Hynix System IC research center in 2003 and his main focus is back-end-of-line (BEOL) interconnection as well as CMOS passive device. He had also experienced the 0.18um analog/mixed-signal product development in MagnaChip Semiconductor, spin-off from Hynix until 2011. Soon-Wook Kim obtained a master degree in 1999 and PhD in 2003, both in Material Science and Engineering from Hanyang University (Seoul, Korea).

Basic considerations to define a proper frontend backend interaction for die bonding

Dr. Evelyn Napetschning received her Ph.D. and master's degrees in technical physics from Vienna University of Technology, Austria in 2008 and 2003 respectively. Dr. Evelyn has 12 years of experience in semiconductors frontend/backend process integration. She is currently a Senior Staff Engineer at Infineon Technologies. She is also holding process block catalogue integration champion and complexity manager position within the TEX complexity management team, Villach (Austria) and Melaka (Malaysia). Dr. Evelyn holds 7 patents to her credit.

Technology Trends for Large Area Panel Level Packaging

Tanja Braun studied mechanical engineering at Technical University of Berlin with a focus on polymers and micro systems and joined Fraunhofer IZM in 1999. Since 2000 she is working with the group Assembly & Encapsulation Technologies and since 2016 she is head of this group. Her field of research is process development of assembly and encapsulation processes, the qualification of these processes using both non-destructive and destructive tools and advanced polymer analysis. Recent research is focused on wafer and panel level packaging technologies and Tanja Braun is leading the Fan-out Panel Level Packaging Consortium at Fraunhofer IZM Berlin. In 2013 she received her Dr. degree from the Technical University of Berlin for the work focusing on humidity diffusion through particle-filled epoxy resins. Results of her research concerning packaging for advanced packages have been presented at multiple international conferences. Tanja Braun holds also several patents in the field of advanced packaging. In 2014 she received the Fraunhofer IZM research award

Jump the Learning Curve: Looking Beyond Cluster Tools for Barrier/Seed Layer PVD

Paul Werbaneth received the B.S. degree in chemical engineering from Cornell University, Ithaca, NY, USA, and recently completed studies in spoken Japanese from the Cornell Summer FALCON Program, and in marketing strategy, also through Cornell. He is Global Product Marketing Director at Intevac, Inc. Paul's writing activities include his frequent contributions on heterogeneous integration and 2.5-D/3-D IC technology and commercialization to the website 3D InCites. He is also a guest editor of IEEE Transactions on Semiconductor Manufacturing; wrote the contributed chapter on TSV etching in the book "3D Integration for VLSI Systems," and has written and presented an extensive number of articles, papers, blogs, and talks regarding the semiconductor capital equipment business

Low temperature interconnect technology using Sn-Bi alloy system for high performance packages

Kei Murayama received his B.E. and M.E. degrees in chemical engineering from Shinshu University, Nagano, Japan in 1991 and 1993, respectively.
He joined SHINKO ELECTRIC INDUSTRIES CO., LTD. in 1993.
He has been engaged in the research and development of semiconductor packaging. He has 25 years of experience in semiconductor packaging industry and has worked in various interconnect techniques and packaging techniques such as solder ball formation, flip chip bonding, TLP bonding, silicon package, silicon interposer, wafer bonding and HS attach.
His current research interests include a low temperature and a low stress bonding for high performance package such as organic interposer. He is mainly working on the development of flip chip bonding technique using low temperature solder and elucidation of its electro-migration phenomenon.

And his current interests also include microstructure and crystal orientation analyses of the interconnection bump by Electron probe micro analyzer (EPMA) and Electron backscattered diffraction (EBSD).

Packaging for Performance Scaling

Sam Karikalan is a Senior Manager at Broadcom Inc., Irvine, California, leading a global team of Signal Integrity, Thermal and Mechanical design experts that is responsible for package design optimization for performance in networking, broadband, storage, wireless and mobile devices. Sam has been with Broadcom for over 13 years. Prior to that, he worked for STATS ChipPAC, Primarion and Advanced Micro Devices on electrical modeling and characterization, package design optimization for electrical performance and component level EMI. The first ten years of Sam's 31 yearlong industry experience was on System Level EMI/EMC at SAMEER-Centre for Electromagnetics in India, being responsible for EMC Compliance Testing, EMI fixes and EMC Design. Besides package design optimization for SI/Thermal/Mechanical performance, Sam is also currently working on Package Technology Development for Performance Scaling, such as 2.5D Integration, extensively working with the supply chain. He has 22 issued US patents and several papers in International Conferences/Journals to his credit. He is a Senior Member of the IEEE and a Member-at-Large on the Board of Governors of the IEEE Electronics Packaging Society. Sam also served as the General Chair of the 2018 IEEE Electronics Components and Technology Conference (ECTC), held in San Diego, California this year

Microfluidic Electroless Interconnection Process for Low-Temperature, Pressure- less Chip-stacking

C. ROBERT KAO (SM'11) received his PhD in Materials Science from University of Wisconsin-Madison in 1994. He joined National Central University (Taiwan) in 1995 as an assistant professor. In 2005, he became the first director for the newly established Graduate Institute of Materials Science & Engineering at National Central University. In 2006 he relocated to National Taiwan University, became a University Distinguished Professor in 2008, and served as the Department Head of Materials Science and Engineering from 2010 to 2013. He currently also serves as the program manager of Materials Engineering in Ministry of Science and Technology of Taiwan. His main research interests include electronic, optical, and MEMS packaging with a main thrust on the thermodynamics and kinetics of materials interactions within packages. He helped organizing 16 international symposia on solders and soldering technology for TMS and ASM. He has served as guest editors for Journal of Electronic Materials and Microelectronic Reliability, and currently is a Principal Editor for Journal of Materials Research and Associate Editor for Journal of Materials Science – Materials in Electronics. Kao is a committee member for CPMT Materials and Processing Technical Committee, and also served as session chair for ECTC meeting.

Kao is a Fellow of the ASM and MRS-Taiwan. In 2014, he received the Brimacombe Medalist Award from TMS. He is a High Impact Research Icon of University of Malaya, Kuala Lumpur.
He has authored over 130 referred journal papers, five of which reached the status of Highly Cited Papers according to Web of Science Essential Science Indicators. He has an h-index of 33. He holds 10 US and Taiwan patents. Kao is considered the leading experts on the metallurgical reactions for electronic packaging applications, and has given more than 30 invited or keynote lectures in international conferences. He presented an invited talk at the Gordon Research Conference (Plymouth State College, July 23-28, 2000), and served as a discussion leader for the same conference in 2006. In addition to his teaching and research activities, Professor Kao was an independent board member of LOTES (2006-2010), and served as consultants for many industry leading corporations, including ASUS and VIA Technologies