**“Emerging NAND Memory Packaging Challenges”**

Dr. Gokul Kumar is a Principal Engineer with the Packaging & Assembly Group at Western Digital, Milpitas, USA. He has a multi-disciplinary expertise in the areas of packaging of electronic systems, signal and power integrity, 3-D integration. Previously, he worked on developing 3-D interposers within the glass/silicon interposer consortia at the 3-D packaging research center in Georgia Tech. He has coauthored about 15 conference and journal publications, with 1 issue patent and 5 others pending. He regularly reviews papers for IEEE CPMT, and several other conferences including EPEPS, International Midwest Symposium on Circuits and Systems, etc.
He received his PhD and MS specializing in Electrical and Computer Engineering, from the Georgia Institute of Technology in 2015 and 2010 respectively.

**“Basic considerations to define a proper frontend backend interaction for die bonding”**

Dr. Evelyn Napetschning received her Ph.D. and master’s degrees in technical physics from Vienna University of Technology, Austria in 2008 and 2003 respectively. Dr. Evelyn has 12 years of experience in semiconductors frontend/backend process integration. She is currently a Senior Staff Engineer at Infineon Technologies. She is also holding process block catalogue integration champion and complexity manager position within the TEX complexity management team, Villach (Austria) and Melaka (Malaysia). Dr. Evelyn holds 7 patents to her credit.

**"Submicron Polymer Re-distribution Layer Technology for Advanced InFO Packaging"**

Han-Ping Pu received Ph.D. degree in Materials Science and Engineering from National Sun Yat-Sen University, Kaohsiung, Taiwan, in 1995. He devoted himself to the field of semiconductor packaging for over 20 years. His career is mainly focus on advanced packaging development, package modeling and resolving chip-package interaction issues. He is now a Deputy Director of Advanced Packaging Division in TSMC R&D, Hsinchu, Taiwan. He has been involved in the invention of over 80 US patents and published more than 10 technical papers in semiconductor packaging area. He is an IEEE and EPS member.

**"Temporary Wafer Bonding Technology for Advanced Packaging"**

Dongshun Bai earned his Ph.D. in Chemical Engineering from Vanderbilt University. In 2007, he joined Brewer Science, Inc., where he has worked as Senior Scientist and Senior Program Manager in the Advanced Technologies R&D group and led the R&D work on temporary bonding and release materials. He is currently the Deputy Business Development Director of the Wafer-Level Packaging Materials business unit at Brewer Science.

**“Advanced Interconnect Material Solutions for 5G Market”**

Yuan Yuan Zhou is the Global Marketing and Business Development Director at Interconnect Solutions, Electronics and Imaging, DowDupont. Interconnect Solutions have over $1B business, providing material solutions for printed circuit board and advanced packaging applied in many market areas such as consumer electronics, automotive, telecommunication and military.

Yuan Yuan joined Dow as a Sr. Manager at Corporate Strategy in Midland, Michigan, who led extensive strategic financial analysis and market assessments for overall Dow portfolio and market participation. She was then named to Global Marketing Director at Electronic Materials leading business integration, portfolio management, and market development. She also led global strategic marketing for automotive interiors in Dow Automotive systems developing overall automotive interior market participation strategy.

Prior to joining Dow, Yuan Yuan was a Sr. development engineer at Intel Assembly & Test Technology development (ATD) located in Chandler, Arizona. She led integration and product qualification process of multiple generation of assembly technology. Yuan-Yuan holds a Ph.D. in Mechanical Engineering from the University of Michigan and a MBA from the Wharton School of Business

**“A Framework for Reliability Assessment of Chemical-Induced Display Delamination”**

Dr. Kedar Hardikar is the Module Reliability Engineering Lead (Mechanical) for products developed by Google’s Consumer Hardware division. In addition, he is an adjunct faculty member at San Jose State University,California.

He holds a Ph.D in Solid Mechanics from the Division of Engineering, Brown University, and has over 10 years of technical leadership experience in semiconductor capital equipment, solar, and consumer electronics industries.
Dr. Hardikar has authored several technical publications and offered invited talks, including an invited paper in JMPS and an invited talk at NIST. Before joining Google, he was the Director of the Reliability Integration Simulation and Certification (RISC) group at Miasole, a global leader in CIGS PV technology.

**"Packaging for Performance Scaling"**

Sam Karikalan is a Senior Manager at Broadcom Inc., Irvine, California, leading a global team of Signal Integrity, Thermal and Mechanical design experts that is responsible for package design optimization for performance in networking, broadband, storage, wireless and mobile devices. Sam has been with Broadcom for over 13 years. Prior to that, he worked for STATS ChipPAC, Primarion and Advanced Micro Devices on electrical modeling and characterization, package design optimization for electrical performance and component level EMI. The first ten years of Sam's 31 yearlong industry experience was on System Level EMI/EMC at SAMEER-Centre for Electromagnetics in India, being responsible for EMC Compliance Testing, EMI fixes and EMC Design. Besides package design optimization for SI/Thermal/Mechanical performance, Sam is also currently working on Package Technology Development for Performance Scaling, such as 2.5D Integration, extensively working with the supply chain. He has 22 issued US patents and several papers in International Conferences/Journals to his credit. He is a Senior Member of the IEEE and a Member-at-Large on the Board of Governors of the IEEE Electronics Packaging Society. Sam also served as the General Chair of the 2018 IEEE Electronics Components and Technology Conference (ECTC), held in San Diego, California this year.

**"ESD, EOS and AMR"**

Stevan Hunter, PhD, is Reliability Engineering Consultant and ESD Control Champion at ON Semiconductor in Phoenix, Arizona, USA, with 40 years of experience in Semiconductor engineering. He also manages university research projects for ON, and teaches as Faculty Associate at ASU, BYU-Idaho and UMD CALCE.

**"Technology Trends for Large Area Panel Level Packaging"**

Tanja Braun studied mechanical engineering at Technical University of Berlin with a focus on polymers and micro systems and joined Fraunhofer IZM in 1999. Since 2000 she is working with the group Assembly & Encapsulation Technologies and since 2016 she is head of this group. Her field of research is process development of assembly and encapsulation processes, the qualification of these processes using both non-destructive and destructive tools and advanced polymer analysis. Recent research is focused on wafer and panel level packaging technologies and Tanja Braun is leading the Fan-out Panel Level Packaging Consortium at Fraunhofer IZM Berlin. In 2013 she received her Dr. degree from the Technical University of Berlin for the work focusing on humidity diffusion through particle-filled epoxy resins. Results of her research concerning packaging for advanced packages have been presented at multiple international conferences. Tanja Braun holds also several patents in the field of advanced packaging. In 2014 she received the Fraunhofer IZM research award

**"Low temperature interconnect technology using Sn-Bi alloy system for high performance packages"**

Kei Murayama received his B.E. and M.E. degrees in chemical engineering from Shinshu University, Nagano, Japan in 1991 and 1993, respectively.
He joined SHINKO ELECTRIC INDUSTRIES CO., LTD. in 1993.
He has been engaged in the research and development of semiconductor packaging. He has 25 years of experience in semiconductor packaging industry and has worked in various interconnect techniques and packaging techniques such as solder ball formation, flip chip bonding, TLP bonding, silicon package, silicon interposer, wafer bonding and HS attach.
His current research interests include a low temperature and a low stress bonding for high performance package such as organic interposer. He is mainly working on the development of flip chip bonding technique using low temperature solder and elucidation of its electro-migration phenomenon.
And his current interests also include microstructure and crystal orientation analyses of the interconnection bump by Electron probe micro analyzer (EPMA) and Electron backscattered diffraction (EBSD).

**"Microfluidic Electroless Interconnection Process for Low-Temperature, Pressureless Chip-stacking"**

C. ROBERT KAO (SM'11) received his PhD in Materials Science from University of Wisconsin-Madison in 1994. He joined National Central University (Taiwan) in 1995 as an assistant professor. In 2005, he became the first director for the newly established Graduate Institute of Materials Science & Engineering at National Central University. In 2006 he relocated to National Taiwan University, became a University Distinguished Professor in 2008, and served as the Department Head of Materials Science and Engineering from 2010 to 2013. He currently also serves as the program manager of Materials Engineering in

Ministry of Science and Technology of Taiwan. His main research interests include electronic, optical, and MEMS packaging with a main thrust on the thermodynamics and kinetics of materials interactions within packages. He helped organizing 16 international symposia on solders and soldering technology for TMS and ASM. He has served as guest editors for Journal of Electronic Materials and Microelectronic Reliability, and currently is a Principal Editor for Journal of Materials Research and Associate Editor for Journal of Materials Science – Materials in Electronics. Kao is a committee member for CPMT Materials and Processing Technical Committee, and also served as session chair for ECTC meeting.
Kao is a Fellow of the ASM and MRS-Taiwan. In 2014, he received the Brimacombe Medalist Award from TMS. He is a High Impact Research Icon of University of Malaya, Kuala Lumpur. He has authored over 130 referred journal papers, five of which reached the status of Highly Cited Papers according to Web of Science Essential Science Indicators. He has an h-index of 33. He holds 10 US and Taiwan patents. Kao is considered the leading experts on the metallurgical reactions for electronic packaging applications, and has given more than 30 invited or keynote lectures in international conferences. He presented an invited talk at the Gordon Research Conference (Plymouth State College, July 23-28, 2000), and served as a discussion leader for the same conference in 2006. In addition to his teaching and research activities, Professor Kao was an independent board member of LOTES (2006-2010), and served as consultants for many industry leading corporations, including ASUS and VIA Technologies

**"Jump the Learning Curve: Looking Beyond Cluster Tools for Barrier/Seed Layer PVD"**

Paul Werbaneth received the B.S. degree in chemical engineering from Cornell University, Ithaca, NY, USA, and recently completed studies in spoken Japanese from the Cornell Summer FALCON Program, and in marketing strategy, also through Cornell. He is Global Product Marketing Director at Intevac, Inc. Paul's writing activities include his frequent contributions on heterogeneous integration and 2.5-D/3-D IC technology and commercialization to the website 3D InCites. He is also a guest editor of IEEE Transactions on Semiconductor Manufacturing; wrote the contributed chapter on TSV etching in the book "3D Integration for VLSI Systems," and has written and presented an extensive number of articles, papers, blogs, and talks regarding the semiconductor capital equipment business

**"Effects of Aging on the Reliability of Electronic Products Incorporating Lead Free Solders"**

Jeffrey C. Suhling received his Ph.D. degree in Engineering Mechanics in 1985 from the University of Wisconsin. He then joined the Department of Mechanical Engineering at Auburn University, where he currently holds the rank of Quina Distinguished Professor and Department Chair. From 2002-2008, he served as Center Director for the NSF Center for Advance Vehicle Electronics. His research interests include solid mechanics, stress and strain analysis, material characterization, experimental mechanics, advanced and composite materials, finite element analysis and computational mechanics, additive manufacturing, electronic packaging, and silicon sensors. Dr. Suhling has authored or co-authored over 400 technical publications, and he has advised over 80 graduate students at Auburn University. He is a Fellow of ASME, and is a member of IEEE, SMTA, IMAPS, SEM, and TAPPI. He served as Chair of the Electrical and Electronic Packaging Division of ASME during 2002-2003, and was on the EPPD Executive Committee from 1998-2003. Dr. Suhling was the Technical Program Chair of the ASME InterPACK '07 Conference, and General Chair of the ASME InterPACK '09 Conference. He currently serves on the IEEE Electronics Packaging Society Board of Governors, and is the General Chair of the 2019 IEEE ITherm Conference

**"Interface Pattern Void Analysis in Face to Face Hybrid Wafer Bonding"**

Soon-Wook Kim is senior process integration engineer at IMEC. He presently performs R&D in the field of hybrid wafer bonding focused on 3D System-On-Chip (SOC) integration for 5 years. Before joining IMEC, he took on the role of 2.5D integration project in Institute of Microelectronics (IME, Singapore). He started the semiconductor various activities at Hynix System IC research center in 2003 and his main focus is back-end-of-line (BEOL) interconnection as well as CMOS passive device. He had also experienced the 0.18um analog/mixed-signal product development in MagnaChip Semiconductor, spin-off from Hynix until 2011. Soon-Wook Kim obtained a master degree in 1999 and PhD in 2003, both in Material Science and Engineering from Hanyang University (Seoul, Korea).

**"Organic substrate material with low transmission loss and effective in suppressing package warpage for 5G application"**

Mr. Shunsuke Tonouchi is currently in Laminate Material R&D Dept., R&D Headquarters, Hitachi Chemical Co., Ltd. He holds Master degree in environmental studies from Tohoku University, Miyagi, Japan, in 2013 after getting Bachelor degree in engineering from Tohoku University, Miyagi, Japan, in 2011. His main study was nanoscience of inorganic chemistry. He has been working in the field of resin design and polymer synthesis for organic substrate material since then.

**"Engineering Green Electronics"**

Dr David Mark Harvey is Professor of Electronic Engineering at Liverpool John Moores University. UK. He conducts research, teaching and enterprise work in digital electronics design, manufacture and test. He has published over 100 articles and successfully supervised 17 PhD students. He has directed two large technology transfer projects funded to €10M, and through these projects worked with over 250 companies. All research work has an industrial bias and the graduates produced have entered industry in the electronics sector. Of three recent PhD graduates, one is European validation manager for a large multinational automotive electronics company, one is working in product validation at Intel in Penang, and a third entered Cambridge Silicon Radio (now Qualcomm). In the past he has helped set up two design centres in India, and worked for companies in the UK in the steel industry, high vacuum scientific instruments and secure electronic communication. His present interests are in the design, manufacture and test of automotive and space electronics.

**“Novel Thin Wafer De-bonding System for 3D TSV Multi-Chip Packaging of High Bandwidth Memory Devices”**

Min Woo Rhee was born in Seoul, South Korea, in 1973. He received the B.Eng. (Hons.), M.Sc., and the Ph.D. degrees in chemical engineering from Sogang University, Seoul, and the master’s degree in management of technology from National University of Singapore (NUS), Singapore. He has about 20 years’ experience in microelectronics packaging research and development for both industry and research institutes. He also has extensive experience in advanced packaging and material development, modeling and characterization. He was also with Amkor Technology Research and Development from 1999 to 2010, where he was the Senior Manager and the Leader of the Material Characterization Modeling and Failure Analysis Group. He also resolved lots of chronic failure and quality issues with the worldwide semiconductor companies. He is currently working as the Program Manager and a Principal Engineer with the Manufacturing Technology Research and Development Center, Samsung Electronics, Hwasung, South Korea. Before his joining Samsung Electronics, he was a Scientist and the Group Leader in interconnection and advanced packaging program (IPP) with the Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR), Singapore. During his working periods in IME A*STAR from 2011 to 2015, he led power module, ruggedized electronics research groups, and industry consortium projects for automotive, oil and gas, deep sea exploration, and aerospace industries. He also has project leading experience on lots of public funded and industry projects related to material and advanced packaging development, such as MEMs, 3-D-IC and fan-out wafer level packaging. In addition, he had developed an automotive three-phase inverter module for power electronics with the Fairchild Semiconductor Research and Development Group as a Principal Engineer, which were successfully implemented for mass production in major automotive industries. He is the author and co-author of 65 journals and conference papers and has more than 20 patents related with microelectronics and advanced packaging area. Also he is the winner of “the Future Creator Award” from Samsung Electronics in 2018 and the “Best Employee of the Year” Award when he was with Amkor in 2009.

**“Opportunities and Challenges of 3D-SiP Heterogeneous Integration Packaging, applied in AI and Autonomous car devices”**

With over 25 years of job experience in SEMI industry, esp. focusing on advanced packaging technologies, such as Bump, FO, 2.5D/3D, SiP, Mr. Albert Lan is a Senior R&D Head of, 13 years of experience in SPIL, which is top 3 biggest assembly house in the world. Prior to this, he was a also PD, Quality, & Sales, 5 years, Amkor Taiwan(Bumping), Vice Chairman of SEMI Taiwan PKG&TEST Committee. Chairman of TILA (Taiwan Intelligent Leader Association). He published more than 50 technical papers and granted more than 30 issued worldwide Patents.