Conference Agenda

20th Electronics Packaging Technology Conference

Date: Tuesday, 04/Dec/2018			
7:30am - 8:30am	**PDC Registration**		
8:30am - 12:00pm	**PDC 1: Introduction to Fan-out Wafer Level Packaging** Location: **Virgo 1** Dr. Beth Keser Director, Packaging Engineering Intel Corporation	**PDC 2: Advanced Integrated Circuit Design for Reliability** Location: **Virgo 2** Dr. Richard Rao Fellow Microsemi Corporation	**PDC 3: 3D SIP For ASIC and DRAM Integration** Location: **Virgo 3** Dr. Li Li Distinguished Engineer Cisco Systems Inc
12:00pm - 1:30pm	**Lunch**		
1:30pm - 5:00pm	**PDC 4: Understanding Flip Chip Technology and Its Applications** Location: **Virgo 1** Mr. Eric Perfecto Principal Member of the Technical Staff GLOBALFOUNDRIES	**PDC 5: Introduction to 3D Interconnect and Packaging Technologies** Location: **Virgo 2** Prof. Sarah Kim Professor Seoul National University of Science and Technology	**PDC 6: Power Electronic Packaging Reliability, Materials, Assembly and Simulation** Location: **Virgo 3** Dr. Ning-Cheng Lee Vice President of Technology, Indium Corporation Dr. Yong Liu Principal Member of Tech Staff, ON Semi Prof. Sheng Liu Dean of the School of Power and Mechanical Engineering and the Institute of Technological Science of Wuhan University

Date: Wednesday, 05/Dec/2018	
7:45am - 8:45am	**Conference Day 1: Registeration**
8:45am - 9:30am	**Conference Opening: Conference Opening** Location: **Leo 1-2-3-4**
9:30am - 10:15am	**Keynote 1** Location: **Leo 1-2-3-4** Mr. Ivor Barber Vice President, Packaging Engineering Advanced Micro Devices
10:15am - 10:45am	**Coffee / Tea Break 1** Location: **Pisces**
10:45am - 11:30am	**Keynote 2** Location: **Leo 1-2-3-4** Dr. Avram Bar-Cohen Principal Engineering Fellow, Raytheon Corporation President, EPS.
11:30am - 12:15pm	**Keynote 3** Location: **Leo 1-2-3-4** Ms Jean Trewhella Director, Packaging Research and Development GLOBALFOUNDRIES.
12:15pm - 1:30pm	**Lunch 1: EPS Luncheon** Location: **Virgo**

1:30pm - 3:30pm	**Plenary Session 1: Heterogeneous Packaging** Location: **Leo 1-2-3-4** Dr. William Chen, ASE Fellow and Senior Technical Advisor, ASE (Moderator) 1. Dr. Gamal Refai-Ahmed, Distinguished Engineer, Xilinx 2. Mr. Mike Delaus, Manager, Analog 3. Mr. Manish Ranjan, Director, Lam Research
3:30pm - 4:00pm	**Coffee / Tea Break 2** Location: **Pisces**
4:00pm - 6:00pm	**Plenary Session 2: Packaging for next generation automobiles/autonomous vehicles** Location: **Leo 1-2-3-4** Dr. Seung Wook Yoon, Director ,JCET (Moderator) 1. Mr. Gaurab Majumdar, Director, Mitsubishi Electric 2. Ms. LC Tan, Sr. Director, NXP Semiconductors 3. Mr. Christophe Bouquet, Director, Infineon Technologies 4. Mr. Santosh Kumar , Director, Yole Development

Date: Thursday, 06/Dec/2018

8:30am - 9:00am	**Invited-01** Location: **Gemini 2** Packaging for Performance Scaling, Mr. Sam Karikalan Broadcom Inc	**Invited-02** Location: **Leo 1** Basic considerations to define a proper frontend backend interaction for die bonding Dr. Evelyn Napetschning Senior Staff Engineer Infineon Technologies	**Invited-03** Location: **Leo 2** Advanced Interconnect Material Solutions for 5G Market Dr. Yuan Yuan Zhou Director DowDupont	**Invited-04** Location: **Leo 3** Emerging NAND Memory Packaging Challenges Dr. Gokul Kumar Principal Engineer Western Digital	**Invited-05** Location: **Leo 4** Microfluidic Electroless Interconnection Process for Low-Temperature, Pressureless Chip-stacking Prof. Robert Kao Professor National Central University (Taiwan)
9:00am - 10:00am	**A-01** Location: **Gemini 2** **P246 - Innovative Packaging Solutions of 3D System in Package with Antenna Integration for IoT and 5G Application** **Mike Tsai, Ryan Chiu, Eric He, J.Y. Chen, Royal Chen, Jensen Tsai, Yu-Po Wang** SPIL, Taiwan	**A-02** Location: **Leo 1** **P284 - Estimation of Maximum Operating Temperature for Cu Wire Bonds: Comparison of Epoxy and Silicone Encapsulant Types** **Stevan G Hunter[1], Michael Hook[2], Michael Mayer[2]** 1: ON Semiconductor, United States of America; 2: University of Waterloo, Canada	**A-03** Location: **Leo 2** **P241 - Suitable Cu leadframe material and design to achieve high reliability requirement and good manufacturability** **Jun{leo} Li, Lidong Zhang, Allen Descartin, Jinmei Liu** NXP Semiconductors, China, People's Republic of	**A-04** Location: **Leo 3** **P127 - Pluggable Silicon Photonics MEMS Switch Package for Data Centre** **How Yuan Hwang** Tyndall National Institute, Ireland	**A-05** Location: **Leo 4** **P305 - Extending the Cooling Limit of Automotive Camera Advanced Driver Assistance Based on Usage Conditions** **Hoa Do, Gamal Refai-Ahmed** Xilinx Inc., United States of America
	A-06 Location: **Gemini 2** **P176 - Concepts for a Monostatic Radar Transceiver Front-end in eWLB Package with Off-Chip Quasi-Circulator for 60 GHz** **Philipp Schmidbauer[1],**	**A-07** Location: **Leo 1** **P247 - High strength bonding on ENIG surface with microporous Ag sintering under a low temperature pressureless condition**	**A-08** Location: **Leo 2** **P205 - Package Integrity and Reliability Effects of Mold Compound Chemistry For Power Device Application** **Matthew M. Fernandez[1], April Joy**	**A-09** Location: **Leo 3** **P206 - Post processing of a SiN-based photonic stack above a CMOS imager sensor** **Nga Phuong Pham, Bert Du Bois, Rita Van Hoof, Gillis Winderickx, Hemant K. Tyagi, Deniz**	**A-10** Location: **Leo 4** **P113 - Thermal simulation and measurement of components in avionics** **Jung Kyun Kim[1], Su Heon Jeong[2]** 1: Mentor, a Siemens Business, Korea, Republic of (South Korea); 2: Defense

	Maciej Wojnowski[2], Robert Weigel[1], Amelie Hagelauer[1] 1: Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany; 2: Infineon Technologies AG	**Zheng Zhang, Chuantong Chen, Katsuaki Suganuma** Institute of Scientific and Industrial Research, Osaka university, Japan	**H. Garete[2], Reinald John S. Roscain[2]** 1: Department of Mining, Metallurgical and Materials Engineering, University of the Philippines - Diliman; 2: Nexperia Philippines, Inc., Philippines	**Sabuncuoglu, Harrie A.C. Tilmans** imec, Belgium	Agency for Technology and Quality
	A-11 Location: **Gemini 2** **P141 - Ceramic Interposers for Ultra-High Density Packaging and 3D Circuit Integration** **Arash Adibi, Aria Isapour, Ammar Kouki** École de technologie supérieure, Canada	**A-12** Location: **Leo 1** **P285 - Cu Sinter Pastes for Pure-Cu Die-Attach Applications of Power Modules** **Barbara Eichinger[1,2], Martin Mischitz[1], Susan Ohm[1,3], Torge Behrendt[4], Fabian Craes[4], Roland Brunner[5]** 1: Infineon Technologies Austria AG, Austria; 2: Department of Physics, University of Graz, Graz, Austria; 3: RWTH Aachen, Aachen, Germany; 4: Infineon Technologies AG Warstein, Germany; 5: Materials for Microelectronics, Material Center Leoben, Leoben, Austria	**A-13** Location: **Leo 2** **P175 - Thermomechanical and Viscoelastic Properties of Dielectric Materials Used in Fan-Out Wafer-Level Packaging** **Yosephine Andriani[1], Xiaobai Wang[1], Songlin Liu[1], Zhaohui Chen[2], Xiaowu Zhang[2]** 1: Institute of Materials Research and Engineering, Singapore; 2: Institute of Microelectronics, Singapore	**A-14** Location: **Leo 3** **P326 - Evaluation of Piezoresistive Polymer-based Traces for Non-invasive Sensor Patch** **Maria Ramona Ninfa B. Damalerio, Ruiqi Lim, Weiguo Chen, David Sze Wai Choong, Ming-Yuan Cheng** Institute of Microelectronics, A-STAR, Singapore	**A-15** Location: **Leo 4** **P126 - Si-based Hybrid Microfluidic Cooling for Server Processor of Data Centre** **Yong Han, Boon Long Lau, Gongyue Tang, Sharon Seow Huang Lim, Xiaowu Zhang** Institute of Microelectronics, A*STAR, Singapore
10:00am - 11:00am	**Tea/Coffee Breaks-03: Interactive Session I and Exhibitor Presentation 1** Location: **Pisces**				
11:00am - 12:20pm	**B-01** Location: **Gemini 2** **P161 - Critical Factors impacting strength of UBM in smaller and denser bumps and methodologies for optimization** **ANANDAN RAMASAMY[1], INDERJIT SINGH[2], SHIN LOW[2], BRYANT LIN[3]** 1: Xilinx Asia Pacific Ltd, Singapore; 2: Xilinx Inc. San Jose, CA 95124, USA; 3:	**B-02** Location: **Leo 1** **P280 - Experimental and Numerical Study on Silicon Die Strength and its Impact on Package Reliability** **Jing-en Luan** STMicroelectronics Pte Ltd, Singapore	**B-03** Location: **Leo 2** **P164 - Solder Resist Crack Resistance Process Characterization in BGA Package for Automotive Grade Reliability** **Kesvakumar V C Muniandy[1], Chan Kheng Jin[1], Peter J.L[2]** 1: Infineon Technologies Asia Pacific Pte Lte, Singapore; 2: Advanced	**B-04** Location: **Leo 3** **P148 - Dual-attached SMT Capacitor Configurations for Small Form Factor and Single-ended Devices** **Chin Lee Kuan[1], Sameer Shekhar[2], Amit K. Jain[2]** 1: Intel Microelectronics, Malaysia; 2: Intel Corporation, Hillsboro, USA	**B-05** Location: **Leo 4** **P112 - Simulation Approach to Predict Warpage based on Resin Curing Behavior during Substrate Manufacturing Process** **MASAHARU FURUYAMA, HIDEAKI NAGAOKA, TOMOYUKI AKAHOSHI** FUJITSU LABORATORIES LTD., Japan

	Xilinx Development Cop. Taiwan Branch		Semiconductor Engineering Group , Kaohsiung, Taiwan		
	B-06 Location: **Gemini 2** **P245 - Development of SiC Chip Based Power Package for High Power and High Performance Application** **GONG YUE TANG, Leong Ching Wai, Teck Guan Lim, Zhaohui Chen, Yong Liang Ye, Pal Singh Ravinder, Lin Bu, Boon Long Lau, Tai Chong Chai, Kazunori Yamamoto, Xiaowu Zhang** Institute of Microelectronics, Singapore	**B-07** Location: **Leo 1** **P211 - Novel concept of an in-situ test system for the thermal-mechanical reliability evaluation of electronic joints** **René Metasch[1], Mike Roellig[1], Uwe Naumann[2], Felix Wiesenhuetter[2], Rainer Kaufmann[3]** 1: Fraunhofer Institute for Ceramic Technologies and Systems IKTS, Germany; 2: Hegewald & Peschke Mess- und Prueftechnik GmbH; 3: Mytron Bio- und Solartechnik GmbH, Germany	**B-08** Location: **Leo 2** **P195 - High bonding strength of silver sintered joints on non-precious metal surfaces by pressure sintering under air atmosphere using micro-silver sinter paste** **Ly May Chew, Wolfgang Schmitt** Heraeus Deutschland GmbH & Co. KG, Germany	**B-09** Location: **Leo 3** **P190 - Wideband slot array antenna for 1 THz band imaging device** **Kota Tsugami, Tanemasa Asano, Haruichi Kanaya** Kyushu University, Japan	**B-10** Location: **Leo 4** **P200 - Numerical Analysis of the Design and Manufacture of Inkjet Printed Electronics Packaging** **Tim Tilford, Stoyan Stoyanov, Chris Bailey** University of Greenwich, United Kingdom
	B-11 Location: **Gemini 2** **P196 - Via Interconnections for Half-Inch Sized Package Fabricated by Minimal Fab** **Fumito Imura[1,2], Michihiro Inoue[1], Sommawan Khumpuang[1,2], Shiro Hara[1,2]** 1: National Institute of Advanced Industrial Science and Technology (AIST), Japan; 2: Minimal Fab Promoting Organization	**B-12** Location: **Leo 1** **P278 - Evaluation of Fatigue Life of BGA Solder by Unsteady Temperature Cycle** **Kento Ogawa** Yokohama National University, Japan	**B-13** Location: **Leo 2** **P260 - Electronic Packaging Solution for 300°C Ambience** **Vivek Chidambaram[1], Eva Wai Leong Ching[2]** 1: Institute of Microelectronics, A*STAR, Singapore; 2: Institute of Microelectronics, A*STAR, Singapore	**B-14** Location: **Leo 3** **P248 - Inter-Chip Data Transfer Capability of TSV-Free Interposer (TFI) Package** **Masaya Kawano, Teck-Guan Lim, Hong-Yu Li** Institute of Microelectronics, A*STAR, Singapore	**B-15** Location: **Leo 4** **P203 - "3rd Level" Solder Joint Reliability Investigations for Transfer of Consumer Electronics in Automotive Use** **Rainer Dudek[1], Marcus Hildebrandt[1], Kerstin Kreyssig[1], Sven Rzepka[1], Ralf Doering[2], Bettina Seiler[2], Thomas Fries[3], Mengjia Zhang[4], Reinhold W. Ortmann[5]** 1: Fraunhofer ENAS, Dept. Micro Materials Center, Chemnitz, Germany; 2: CWM GmbH, Chemnitz, Germany; 3: FRT GmbH, Bergisch-Gladbach, Germany; 4: Robert Bosch GmbH, Automotive Electronics, Reutlingen, Germany; 5: Continental Automotive France SAS, France

	B-16 Location: **Gemini 2** **P274 - Evaluation of Materials for Fan-Out Panel Level Packaging (FOPLP) Applications** **Nagendra Sekhar Vasarla[1], Srinivasa Rao Vempati[1], Kazunori Yamamoto[1], Fujinaga Tetsushi[2], Jono Koichi[3], Matsui Hiroshi[4], Takaya Yoshiteru[3], Yukio Horiguchi[4]** 1: Institute of Microelectronics, Singapore; 2: ULVAC; 3: SCREEN Finetech Solutions Co., Ltd.; 4: SCREEN Semiconductor Solutions	**B-17** Location: **Leo 1** **P122 - Innovative Approach of efficient High Humidity and High Temperature Reverse Bias Testing as significant Qualification Method for Power Electronics Modules** **Martin Mueller, Joerg Franke** Friedrich-Alexander University Erlangen-Nuremberg (FAU), Institute for Factory Automation and Production Systems (FAPS), Germany	**B-18** Location: **Leo 2** **P335 - Mechanical property and plated solder volume effect of Cu core ball** **Jae-Yeol Son[1,2], Seul-Gi Lee[1], Yong-Woo Lee[1], Seung-Boo Jung[2]** 1: MKE, Korea, Republic of (South Korea); 2: Sungkyunkwan University, Korea, Republic of (South Korea)	**B-19** Location: **Leo 3** **P282 - SIPI Co-Sim: Signal Performance of Super Speed Differential I/O with Power Referencing Design** **Li Wern Chew, Paik Wen Ong** Intel Microelectronics (M) Sdn. Bhd., Malaysia	**B-20** Location: **Leo 4** **P230 - Study on Electrical Performance and Mechanical Reliability of Antenna in Package (AIP) with Fan-Out Wafer Level Packaging Technology** **Faxing Che, Zihao Chen** IME, Singapore
12:20pm - 1:50pm	**Lunch-03: Best paper Award, EPTC 2018 committee Appreciation** Location: **Virgo**				
1:50pm - 2:20pm	**Invited-06** Location: **Gemini 2** Submicron Polymer Re-distribution Layer Technology for Advanced InFO Packaging Dr. Han-Ping Pu Deputy Director TSMC	**Invited-07** Location: **Leo 1** A Framework for Reliability Assessment of Chemical-Induced Display Delamination Dr. Kedar Hardikar Module Reliability Engineering Lead Google	**Invited-08** Location: **Leo 2** Temporary Wafer Bonding Technology for Advanced Packaging Dr.Dongshun Bai Deputy Business Development Director Brewer Science.	**Invited-09** Location: **Leo 3** Technology Trends for Large Area Panel Level Packaging Dr.Tanja Braun Assembly & Encapsulation Technologies Head Fraunhofer IZM	**Invited-10** Location: **Leo 4** ESD, EOS and AMR Dr. Stevan Hunter Reliability Engineering Consultant ON Semiconductor
2:20pm - 3:40pm	**C-01** Location: **Gemini 2** **P343 - High density interconnection for heterogenous intergration on FOWLP platform** **Tai Chong Chai, Teck Guan Lim, David Ho, Ser Choong Chong, Faxing Che, Surya Bhattacharya** Institute of Microelectronics, A-STAR, Singapore	**C-02** Location: **Leo 1** **P363 - High-resolution 3D X-ray Microscope for Semiconductor Packages Metrology, Quality and Reliability Assessment** **John Auyoong, Allen Gu** ZEISS Semiconductor Manufacturing Technology, United States of America	**C-03** Location: **Leo 2** **P151 - A study of the growth rate of Cu-Sn intermetallic compounds for transient liquid phase bonding during isothermal aging** **So-Eun Jeong[1,2], Seung-Boo Jung[2], Jeong-Won Yoon[1]** 1: Korea Institute of Industrial Technology (KITECH), Korea, Republic of (South Korea); 2: Department of Advanced Materials Engineering, Sungkyunkwan University, Korea,	**C-04** Location: **Leo 3** **P135 - Dynamic Bending Reliability Analysis of Flexible Hybrid Integrated Chip-Foil Packages** **Nagarajan Palavesam[1,2], Erwin Yacoub-George[1], Waltraud Hell[1], Christof Landesberger[1], Karlheinz Bock[2], Christoph Kutter[1,3]** 1: Fraunhofer EMFT Research Institution for Microsystems and Solid State Technologies, Munich, Germany; 2:	**C-05** Location: **Leo 4** **P213 - High Frequency Power Integrity Design Sensitivity to Package Design Rules** **Sameer Shekhar[1], Amit Kumar Jain[1], Chin Lee Kuan[2]** 1: Intel Corporation, United States of America; 2: Intel Corporation, Malaysia

			Republic of (South Korea)	Electronics Packaging Laboratory, Technische Universität Dresden, Dresden, Germany; 3: Institute of Physics, Universität der Bundeswehr München, Neubiberg, Germany	
	C-06 Location: **Gemini 2** **P129 - Combined Thick Resist Processing and Topography Patterning for Advanced Metal Plating** **Martin Eibelhuber, Johanna Rimböck, Tobias Zenger, Thomas Uhrmann, Thorsten Matthias** EVGroup, Austria	**C-07** Location: **Leo 1** **P221 - Understanding of within Chip variation of optical appearance of Aluminum Pads** **Wei Lee Lim[2], Mario Stefenelli[1], Joel Baldevia Agala[3], Evelyn Napetschnig[1]** 1: Infineon Technologies Austria AG, Austria; 2: Infineon Technologies (Kulim) Sdn. Bhd, Malaysia; 3: Infineon Technologies Batam P.T., Indonesia	**C-08** Location: **Leo 2** **P171 - Dicing Tape Performance in a Plasma Dicing Environment** **Stewart Fulton[1], Oliver Ansell[1], Janet Hopkins[1], Richard Barnett[1], Taku Umemoto[2], Takuo Nishida[2]** 1: SPTS Technologies Ltd, United Kingdom; 2: LINTEC Advanced Technologies (Europe) GmbH	**C-09** Location: **Leo 3** **P349 - Stress-Free Aondic Bonding Technology with SW-YY Glass in Comparison to Common Used Borosilicate Glass for Sensitive MEMS** **Xiaodong Hu[1,4], Piotr Mackowiak[2], Manuel Baeuscher[1,2], Yucheng Zhang[1,2], Bei Wang[3], Ulli Hansen[4], Simon Maus[4], Oliver Gyenge[4], Oswin Ehrmann[1,2], Klaus-Dieter Lang[1,2], Ha-Duong Ngo[1,3]** 1: Technische Universität Berlin, Germany; 2: Fraunhofer Institute for Reliability and Microintegration, Germany; 3: University of Applied Sciences Berlin, Germany; 4: MSG Lithoglas GmbH, Berlin, Germany	**C-10** Location: **Leo 4** **P302 - Impedance Characterization of Power Delivery Network in a Flip Chip Package on a Printed Circuit Board** **Suat Mooi Low, Fei Guo, Wui Weng Wong** AMD, Singapore
	C-11 Location: **Gemini 2** **P198 - Design Optimization of Through-Silicon Vias for Substrate-Integrated Waveguides embedded in High-Resistive Silicon Interposer** **Matthias Wietstruck[1], Steffen Marschmeyer[1], Selin Tolunay Wipf[1], Christian Wipf[1], Thomas Voß[1], Matthieu Bertrand[3], Emmanuel Pistono[4],**	**C-12** Location: **Leo 1** **P142 - High-resolution Time-domain Reflectometry Analysis in Back-end-of-line (BEOL) by Recursive Circuit Modelling** **Yang Shang[1], Makoto Shinohara[2], Rahul Babu Radhamony[3], Joanna Kiljan[3], Alan Wu[3]** 1: Advantest (Singapore) Pte Ltd, Singapore; 2:	**C-13** Location: **Leo 2** **P202 - Low Transmission Loss Polyimides Substrates: A Novel Alternative to Liquid crystal polymers** **Takashi Tasaki** ARAKAWA CHEMICAL INDUSTRIES, LTD., Japan	**C-14** Location: **Leo 3** **P192 - Guided Interconnect – The Next-Generation Flex Circuits for High-Performance System Design** **Jackson Kong, Bok Eng Cheah, Khang Choong Yong, Stephen Hall, Eric Gantner, Chaitanya Sreerama** Intel Corporation	**C-15** Location: **Leo 4** **P110 - Wafer Level Reliability Characterization of 2.5D IC packages** **Jayasanker Jayabalan, Jong Ming Chinq, Vivek Chidambaram Nachiappan, Sharon Lim Pei Siang, Calvin Chua Hung Ming, Surya Bhattacharya** Institute of Microelectronics, Singapore

	Giuseppe Acri[4], Florence Podevin[4], Philippe Ferrari[4], Mehmet Kaynak[1,2] 1: IHP, Germany; 2: Sabanci University, Turkey; 3: Laboratoire d'Electronique et Electromagnetisme, Sorbonne Universite, France; 4: RFIC-Lab, COMUE University, France	Advantest Corporation, Japan; 3: Qualcomm, Inc., USA			
	C-16 Location: **Gemini 2** **P240 - Comprehensive study on die shift and die protrusion issues during molding process of Mold-1st FOWLP** **SIAK BOON LIM, Ser Choong Chong, Sharon Pei Siang Lim, Wen Wei Seit, Xiaowu Zhang** IME, Singapore	**C-17** Location: **Leo 1** **P111 - Accelerated Moisture Soak for Moisture Sensitivity Analysis Revisited** **ATCHAREEYA AREE-UEA, AMAR MAVINKURVE, MICHIEL VAN SOESTBERGEN, RENE RONGEN, Leo {Jun} Li** NXP Manufacturing (Thailand) Ltd, Thailand	**C-18** Location: **Leo 2** **P249 - the study of void formation in Ag sinter joint** **ruifen zhang, lingling teo, Dennis Ang** heraeus material singapore, Singapore	**C-19** Location: **Leo 3** **P275 - Integrated Magnetic Inductor Technology on Silicon** **Salahuddin Raju[1], Serine Soh[1], Leong Yew Wing[1], David Ho[1], Lin Huamao[1], Marco Stenger Koob[2], Jerzy Wrona[2], Matthias Landmann[2], Berthold Ocker[2], Jürgen Langer[2], Ravinder Pal Singh[1]** 1: Institute of Microelectronics, A*STAR, Singapore; 2: Singulus Technologies, Kahl am Main, Germany	**C-20** Location: **Leo 4** **P182 - Accurate Modeling Method of LGA Package for High Power Application** **Cheng-Yu Tsai** Advanced Semiconductor Engineering, Inc, Taiwan
3:40pm - 4:40pm	**Tea/Coffee Breaks-04: Interactive Session 1 and Exhibitor Presentation 2** Location: **Pisces**				
4:40pm - 6:00pm	**D-01** Location: **Gemini 2** **P204 - Stabilizing Flow Boiling Operation of a Microchannel Heat Sink using a Hybrid Geometric Configuration** **John Mathew, Poh Seng Lee, Wu Tianqing, Christopher Yap** National University of Singapore, Singapore	**D-02** Location: **Leo 1** **P283 - An Evaluation of the Electrical Stability of Copper Filled Isotropic Conductive Adhesives in High Moisture Environments** **Shanda Wang, David Hutt, David Whalley, Gary Critchlow** Loughborough University, United Kingdom	**D-03** Location: **Leo 2** **P225 - Laser Separation of Dissimilar Substrates Using Water Washable Materials** **John Cleaon Moore[1], Stefan Quandt[2]** 1: Daetec LLC, United States of America; 2: Trumpf, Inc., United States of America	**D-04** Location: **Leo 3** **P237 - Magnetic Shielding and Packaging of STT MRAM** **Teck Guan Lim[1], Boo Yang Jung[2], Leong Ching Wai[1]** 1: Institute of Microelectronics, Singapore; 2: GLOBALFOUNDRIES Singapore Pte Ltd	**D-05** Location: **Leo 4** **P207 - Processing Models Based on Stress Conservation Law Utilized for Temperature-Dependent Warpage Prediction of MUF FCCSP with 3L ETS** **Chih-Sung Chen, Nicholas Kao, Poyu Liao, Ssu-Cheng Lai, Don Son Jiang** Siliconware Precision Industries Co. Ltd., Taiwan
	D-06 Location: **Gemini 2**	**D-07** Location: **Leo 1**	**D-08** Location: **Leo 2**	**D-09** Location: **Leo 3**	**D-10** Location: **Leo 4**

	P348 - Comparison of temperature distributions in modern nanostructures based on different parameters of Dual-Phase-Lag equation **Tomasz Raszkowski, Agnieszka Samson, Mariusz Zubert** Lodz University of Technology, Poland	**P332 - Cracking failure of Cu pillar bump caused by electromigration and stress concentration under thermo-electric coupling loads** **Si Chen, Bin Zhou, Zhizhe Wang, Yunfei En, Yun Huang, Bin Yao** China electronic product reliability and environmental testing research institute, China, People's Republic of	**P257 - Enhancing Productivity for IC-substrate manufacturing by using a novel Copper Electrolyte for Semi Additive Plating** **Mustafa Özkök[1], Olivier Mann[1], Toshiya fujiwara[2]** 1: Atotech Deutschland GmbH, Germany; 2: Atotech Japan K.K.	**P170 - Implementation of High-Temperature Pressure Sensor Package and Characterization up to 500 °C** **Nilavazhagan Subbiah[1], Qingming Feng[1], Kevin Ali Beltran Ramirez[1], Jürgen Wilde[1], Gudrun Bruckner[2]** 1: IMTEK, University of Freiburg, Germany; 2: CTR AG, HIT Villach, Austria	**P234 - Solder Joint Reliability Simulation of Fan-out Wafer Level Package Considering Visco-Elastic Material Properties** **ZHAOHUI CHEN** IME A-Star, Singapore, Singapore
	D-11 Location: **Gemini 2** **P133 - Modeling and Control of Hybrid Si-Based Micro-Fluid Cooling System for Data Center Application** **Haoran Chen, Yong Han, Gongyue Tang, Xiaowu Zhang** IME A*STAR, Singapore	**D-12** Location: **Leo 1** **P187 - Research on the effect of bonding properties of micro bumps for different morphology and interconnection methods** **Fengwei Dai[1,2,3], David Wei Zhang[1], Meiying Su[2,3], Guojun Wang[3], Dengfeng Yang[3], Wenqi Zhang[2,3], Liqiang Cao[2,3]** 1: School of Microelectronics, Fudan University; 2: Institute of microelectronics of Chinese academy of sciences; 3: The National Center for Advanced Packaging, China, People's Republic of	**D-13** Location: **Leo 2** **P288 - Isoconversional Method for the Modeling of the Curing Kinetics of Epoxy Molding Compounds for Mold Process Simulation** **Tamas Deak[1], David O. Kazmer[2]** 1: Philips Lighting Hungary Kft., Hungary; 2: University of Massachusetts Lowell	**D-14** Location: **Leo 3** **P128 - Multilayer Roll-to-Roll Screen-Printing for Printed Electronics Applications** **Budiman Salam, X.C Shan, Zhanhong Cen, B.K. Lok** Singapore Institute of Manufacturing Technology, Singapore	**D-15** Location: **Leo 4** **P181 - Numerical analysis of laser thermal compression bonding for flip chip package** **Youngmoon Jang[1], Byoung-Ho Ko[1], Hoon Sun Jung[2], Jin Wook Jeong[3], Sung-Hoon Choa[2]** 1: Dept. Of Manufacturing System and Design Engineering Seoul National University of Science and Technology, Seoul.; 2: Graduate School of Nano IT Design Fusion, Seoul National University of Science and Technology, Seoul, 01811, Republic of Korea; 3: R&D Center New Product Development team, HANA Micron Inc, Seongnam-Si, Korea
	D-16 Location: **Gemini 2** **P159 - Spray cooling enhancement studies using dielectric liquid** **Ranjith Kandasamy, Pengfei Liu, Huicheng Feng, Teck**	**D-17** Location: **Leo 1** **P355 - Fine Pitch Cu to Cu interconnects for 2.5D Packaging** **Ling Xie, Ser Choong Chong, Vasarla Nagendra Sekhar, Daniel**	**D-18** Location: **Leo 2** **P255 - Phthalonitrile (PN) based electronic packages for High Temperature Applications** **Eric Jian Rong Phua[1,2], Ming Liu[3], Jacob Song Kiat**	**D-19** Location: **Leo 3** **P163 - Fabrication and Packaging of surface electrode ion trap for quantum computing**	**D-20** Location: **Leo 4** **P334 - Warpage prediction and stress analysis for large size through-silicon-via interposer package**

	Neng Wong, Kok Chuan Toh School of Mechanical and Aerospace Engineering, Nanyang Technological University, Singapore	**Ismael Cereno, Sunil Wickramanayaka** Institute of Microelectronics, A*STAR, Singapore	**Lim[1,3], Bokun Cho[4], Chee Lip Gan[1,3]** 1: School of Materials Science and Engineering; 2: School of Chemical and Biomedical Engineering; 3: Temasek Laboratories@NTU; 4: Energetics Research Institute	**Jing Tao, Nam Piau Chew, Chuan Seng Tan** Nanyang Technological University, Singapore	**Meiying Su[1,2], Jun Li[1,2], Liqiang Cao[1,2]** 1: Institute of Microelectronics of the Chinses Academy of Sciences, China, People's Republic of; 2: National Center for Advanced Packaging Co., Ltd
6:30pm - 9:30pm	**Conference Banquet: Conference Banquet**				

Date: Friday, 07/Dec/2018

8:30am - 9:00am	**Invited 11** Location: **Gemini 2** Interface Pattern Void Analysis in Face to Face Hybrid Wafer Bonding Dr Soon-Wook Kim Senior Engineer IMEC	**Invited 12** Location: **Leo 1** Engineering Green Electronics Prof. David Mark Harvey Professor Liverpool John Moores University	**Invited 13** Location: **Leo 2** Organic substrate material with low transmission loss and effective in suppressing package warpage for 5G application Mr. Shunsuke Tonouchi Hitachi Chemicals	**Invited 14** Location: **Leo 3** Electronic Materials and Packaging Trends in the Era of Digital Transformation Ms.Rozalia Beica Global Director Strategic Marketing DowDupont	**Invited 15** Location: **Leo 4** Thermal and Failure Analysis of Advanced Sub-Micron Devices Using Transient Thermoreflectance Thermography Prof. Andrew Tay Adjunct Fellow Singapore University of Technology and Design
9:00am - 10:20am	**E-01** Location: **Gemini 2** **P319 - Development of cost effective Copper overburden removal for Via-Last TSV fabrication** **QIN REN, WOON LENG LOH, XIANG YU WANG** Institue of Microelectronics, A*star, Singapore	**E-02** Location: **Leo 1** **P149 - Develop Smart Wire Bonding Processes for Smart Factories** **Ivy Qin, Aashish Shah, Basil Milton, Gary Schulze, Nelson Wong, Andrew Chang** kulicke and soffa ind. inc, United States of America	**E-03** Location: **Leo 2** **P172 - In-situ Cure Shrinkage Characterization of Epoxy Molding Compounds for FOWLP** **Xiaobai Wang[1], Yosephine Andriani[1], Songlin Liu[1], Zhaohui Chen[2], Xiaowu Zhang[2]** 1: Institute of Materials Research and Engineering, A* Star, Singapore; 2: Institute of Microelectronics, A* star, Singapore	**E-04** Location: **Leo 3** **P329 - Development of Three Dimensional Roll-up Polymer-Si Structure for Nerve Ablation Catheter** **Ruiqi Lim, Weiguo Chen, David Sze Wai Choong, Maria Ramona Damalerio, Ming-Yuan Cheng** Institute of Microelectronics, Singapore	**E-05** Location: **Leo 4** **P268 - LED multiphysics modelling for "Industry 4.0", an approach proposed by the Delphi4LED European project** **Marta Rencz[1,2], Gabor Farkas[1], Lajos Gaal[1], Andras Poppe[1,2], Robin Bornoff[3]** 1: Mentor Graphics, Hungary; 2: Budapest University of Technology and Economics, Hungary; 3: Mentor Graphics, UK
	E-06 Location: **Gemini 2** **P153 - One Micron Damascene Redistribution for Fan-Out Wafer Level Packaging using a Photosensitive**	**E-07** Location: **Leo 1** **P123 - Investigations of Silver Sintered Interconnections on 3-Dimensional Ceramics with Plasma Based Additive Copper Metallizations**	**E-08** Location: **Leo 2** **P217 - Resolving Plating, stripping, etching challenges for shrinking dimension in advanced packaging**	**E-09** Location: **Leo 3** **P185 - Highly Stretchable, Durable, and Printable Textile Conductor** **Won Jae Lee[1], Jin Yeong Park[1], Hyun Jin Nam[2], Sung-Hoon Choa[1]**	**E-10** Location: **Leo 4** **P209 - Experimental Study of Ageing Effect in Pool Boiling Heat Transfer** **Tianqing Wu, Poh Seng Lee, John Mathew, Si Rong Lu** National University of Singapore, Singapore

	Dielectric Material **Robert Hsieh[1], Warren W Flack[1], Ha-Ai Nguyen[1], John Slabbekoorn[2], Samuel Suhard[2], Andy Miller[2], Akito Hiro[3], Romain Ridremont[3]** 1: Ultratech, a division of Veeco; 2: IMEC; 3: JSR MICRO NV	**Alexander Hensel[1], Christian Schwarzer[2], Matthias Scheetz[1], Michael Kaloudis[2], Joerg Franke[1]** 1: Friedrich-Alexander University Erlangen-Nürnberg, Germany; 2: Aschaffenburg University of Applied Science	**KOK GUAN NG, Jerome DAVIOT** TECHNIC ASIA PACIFIC PTE LTD, Singapore	1: Graduate School of Nano IT Design Fusion, Seoul National University of Science and Technology, Seoul, 01811, Republic of Korea; 2: Dept. Of Manufacturing System and Design Engineering Seoul National University of Science and Technology, Seoul, 01811, Republic of Korea	
	E-11 Location: **Gemini 2** **P208 - The Robust WLCSPs : enabling 5-side protection** **Seung YOON[1], Tony Chen[2]** 1: Statschippac PTE LTD, JCET Group, Singapore; 2: JCAP, JCET Gorup, China	**E-12** Location: **Leo 1** **P174 - Low-temperature Cu-Cu bonding by self-reduction of particle-free Ag ion paste** **Junjie Li, Tielin Shi, Guanglan Liao, Zirong Tang** Huazhong University of Science and Technology, China, People's Republic of	**E-13** Location: **Leo 2** **P361 - Preparation and mechanical characterization of Ni-Fe-P coating for power electronics** **Li Liu[2], Juan Peng[2], Sheng Liu[1], Zhiwen Chen[1]** 1: Wuhan University, China, People's Republic of; 2: Wuhan University of Technology, China, People's Republic of	**E-14** Location: **Leo 3** **P331 - Development of a Flexible Printed Multi-Functional Sensor Platform for Medical Applications** **David Choong, Ruiqi Lim, Maria Ramona, Weiguo Chen, Ming Yuan Cheng** ASTAR Institute of Microelectronics, Singapore	**E-15** Location: **Leo 4** **P228 - Design, Fabrication and Characterization of a Compact Mini Heat Exchanger for Data Centre Cooling Applications** **GONG YUE TANG, Yong Han, Haoran Chen, Xiaowu Zhang** Institute of Microelectronics, Singapore
	E-16 Location: **Gemini 2** **P239 - Process Development of Fan-Out interposer with Multi-layer RDL for 2.5D System in Package** **HSIANG-YAO HSIAO, Soon Wee Ho, Siak Boon Lim, Ser Choong Chong, Pei Siang Lim, Tai Chong Chai** Astar-IME, Singapore	**E-17** Location: **Leo 1** **P338 - New Alternative Metal Coated Silver bonding wire for Gas-Free bonding and High Reliability Performance** **SangYeob Kim, SungMin Jeon, ChongMin Park, ByungHoon Jung, SeungHyoun Kim, JeongTak Moon** MK Electron Co., Ltd, Korea, Republic of (South Korea)	**E-18** Location: **Leo 2** **P266 - Effect of the Strengthening Mechanism on the Response of a Solder Alloy to Strain Rate and Ageing** **Wayne Chee Weng Ng[1], Tetsuya Akaiwa[1], Pavithiran Narayanan[2], Keith Sweatman[1], Tetsuro Nishimura[1], Takatoshi Nishimura[1]** 1: Nihon Superior Co., Ltd., Japan; 2: Nihon Suuperior (M) Sdn. Bhd.	**E-19** Location: **Leo 3** **P328 - Molecular Dynamics Simulation of GaN Nano-grinding** **Yixin Xu[1], Fulong Zhu[1], Miaocao Wang[1], Xiaojian Liu[1], Sheng Liu[2]** 1: Huzahong University of Science and Technology, People's Republic of China; 2: Wuhan University, People's Republic of China	**E-20** Location: **Leo 4** **P254 - A Low Computational Cost and Accurate Thermal Calculation Method for Multi-hotspot IC** **Daixing Wang[1], Yudan Pi[1,2], Wei Wang[2,3], Yufeng Jin[1,2,3]** 1: School of Electronic and Computer Engineering, Peking University Shenzhen Graduate School, Shenzhen, Guangdong, China; 2: Institute of Microelectronics, Peking University, Beijing, China; 3: National Key Lab of Micro/Nano Fabrication Technology, Peking University, Beijing, China 1 dxwang1215@pku.edu.cn; * w.wang@pku.edu.cn

10:20am - 11:10am	**Tea/Coffee Breaks-05: Interactive Session 2 / Exhibitor Presentation 3** Location: **Pisces**				
11:10am - 12:30pm	**F-01** Location: **Gemini 2** **P295 - Extending cooling limit of RRU based on level 1 thermal management** **Gamal Refai-Ahmed, Hoa Do, Brian Philofsky, Anthony Torza** Xilinx Inc., United States of America	**F-02** Location: **Leo 1** **P262 - Enhancing Bump Thick Resist Lithography: Establishing Process Controls to Eliminate Copper Pillar Footing** **Jose Arvin Matute Plomantes, Ruby Ann Dizon Mamangun, Armando Tresvalles Clarina Jr., Jamel Penuliar Cayabyab, Rafael Jose L. Guevara** Texas Instruments Phils, Philippines	**F-03** Location: **Leo 2** **P238 - Process Development of micro-bump flip chip bonding with Non-Conductive Film** **Ser Choong Chong, Hongyu Xie, Ling Xie, Daniel Ismael Cereno** Institute of Microeclectronics, Singapore	**F-04** Location: **Leo 3** **P253 - K-band SATCOM Receiver Modules: System Design, Analysis and Test using the M3-Approach** **Christian Tschoban, Ivan Ndip** Fraunhofer IZM, Germany	**F-05** Location: **Leo 4** **P298 - Design of Micro-sensors for Measuring Localised Stresses during Fan-Out Wafer Level Packaging (FOWLP) Processes** **Xiaowu Zhang, Zhaohui Chen, Boon Long Lau, Yong Han, Sharon Pei Shang Lim, Simon Siak Boon Lim** Institute of Microelectronics, Singapore
	F-06 Location: **Gemini 2** **P333 - A novel double-layered heat sink for high power electronics** **Yicang Huang[1], Hui Li[1], Shengnan Shen[1], Shiyue Ma[2]** 1: Wuhan University, China, People's Republic of China; 2: Tongji University, China, People's Republic of China	**F-07** Location: **Leo 2** **P188 - Millimeter Wave Antenna in Package (AiP) Measured in Far-Field by a Vertical Probe Station** **Bo-Siang Fang[1], Kuan-Ta Chen[1], Cha-Chu Lai[1], Jui-Ching Cheng[2]** 1: Siliconware Precision Industries Co., Ltd., Taiwan; 2: National Taipei University of Technology	**F-08** Location: **Leo 3** **P354 - Modeling and simulation of chemical amplification photoresist to produce high-density cone-shaped micro bumps** **Daiki Kumagawa, Mamoru Sakamoto, Yohei Aoki, Tanemasa Asano** Kyushu University, Japan	**F-09** Location: **Leo 3** **P304 - Crystal Oscillator Interconnect Architecture with Noise Immunity** **Raymond Chong, Khang Choong Yong** Intel Microelectronics Sdn Bhd, Malaysia	**F-10** Location: **Leo 4** **P232 - Mechanical Characterization of MEMS-Microphones by means of Nanoindentation and Coupled Finite Element Analysis** **Jan Albrecht[1], Marie Weissbach[1], Matthias Vobl[2], Ulrich Krumbein[2], Sven Rzepka[1]** 1: Fraunhofer Institute for Electronic Nano Systems ENAS, Technologie-Campus 3, 09126 Chemnitz, Germany; 2: Infineon Technologies, Am Campeon 1-15, 85579 Neubiberg, Germany
	F-11 Location: **Gemini 2** **P242 - Mold Flow Simulation for Fan-out Panel-Level Packaging (FOPLP)** **Lin Bu** IME, Singapore	**F-12** Location: **Leo 1** **P357 - Critical Surface Quality inspection and analysis of precision optical components fabricated using CMP methods** **venkata ramana pamidighantam[1], MAHENDER**	**F-13** Location: **Leo 2** **P244 - Material Selection for Ion Trap Chip Working at Extreme Low Temperatures** **Lin Bu** IME, Singapore	**F-14** Location: **Leo 3** **P306 - Cost Effective Capacitive Testing for RDL First** **Keita Gunji, Toshihisa Hibarino** Nidec Read Corporation, Japan	**F-15** Location: **Leo 4** **P173 - Dynamic Mechanical Analysis and Viscoelastic Behavior of Epoxy Molding Compounds for FOWLP** **Xiaobai Wang[1], Yosephine Andriani[1], Songlin Liu[1], Zhaohui Chen[2], Xiaowu Zhang[2]** 1: Institute of Materials Research and

		KUMAR GUPTA[2], krishna rao guntuku[2] 1: vasavi college of engineering, HYDERABAD India; 2: ELECTRO OPTICAL INSTRUMENTS RESEARCH ACADEMY, HYDERABAD, INDIA			Engineering, A* Star, Singapore; 2: Institute of Microelectronics, A* star, Singapore
	F-16 Location: **Gemini 2** **P336 - Electromigration Modeling for 3D-IC TSV Interconnect considering grain structure** **Yuanxiang Zhang, Sijia Yu, Deqi Su, Zhipeng Shen** Quzhou University, China, People's Republic of	**F-17** Location: **Leo 1** **P364 - Wafer Level Through-polymer Optical Vias (TPOV) Enabling High Throughput of Optical Windows Manufacturing** **Johan Hamelink** Boschman Technologies, Netherlands, The	**F-18** Location: **Leo 2** **P311 - Gold Passivated Cu-Cu Bonding At 140˚C For 3D IC Packaging And Heterogeneous Integration Applications.** **Satish Bonam, Hemanth Kumar Cheemalamarri, Siva Rama Krishna Vanjari, Shiv Govind Singh** Indian Institute of Technology Hyderabad, India	**F-19** Location: **Leo 3** **P134 - Simulation And Electrical Characterization Of A Novel 2D-Printed Incontinence Sensor With Conductive Polymer PEDOT:PSS For Medical Applications** **Manuel Baeuscher[1,2], Xiaodong Hu[2], Piotr Mackowiak[1], Oswin Ehrmann[1], Klaus-Dieter Lang[1,2], Ha-Duong Ngo[1,3]** 1: Fraunhofer Institute for Reliability and Microintegration Berlin; 2: Technical University Berlin; 3: University of Applied Sciences Berlin	**F-20** Location: **Leo 4** **P199 - Constitutive Behaviour of Single Lap Joint of Sintered Silver Paste** **Xu Long[1], Chongyang Du[1], Wenbin Tang[1], Yongchao Liu[2], Yao Yao[1], Fengrui Jia[3]** 1: School of Mechanics, Civil Engineering and Architecture, Northwestern Polytechnical University, Xi'an, China; 2: College of Mining Engineering, Liaoning Shihua University, Fushun, China; 3: College of Petroleum Engineering, Liaoning Shihua University, Fushun, China
12:30pm - 1:30pm	**Lunch 04** Location: **Virgo** EPTC 2019 Announcement Sponsors Appreciation				
1:30pm - 2:00pm	**Invited 16** Location: **Gemini 2** Novel Thin Wafer De-bonding System for 3D TSV Multi-Chip Packaging of High Bandwidth Memory Devices Dr. Minwoo Daniel Rhee Program Manager Samsung Electronics	**Invited 17** Location: **Leo 1** Low temperature interconnect technology using Sn-Bi alloy system for high performance packages Mr.Kei Murayama SHINKO Electric Industries	**Invited 18** Location: **Leo 2** Effects of Aging on the Reliability of Electronic Products Incorporating Lead Free Solders Prof. Jeff Suhling Professor Auburn University	**Invited 19** Location: **Leo 3** Package Level Systems Integration: A key to maintaining the pace of progress Dr.Bill Bottoms Chairman Third Millennium Test Solutions	**Invited 20** Location: **Leo 4** Opportunities and Challenges of 3D-SiP Heterogeneous Integration Packaging, applied in AI and Autonomous car devices Mr.Albert Lan Global Packaging Director Applied Material Inc
2:00pm - 3:20pm	**G-01** Location: **Gemini 2** **P316 - EPIC Via Last on SOI wafer integration challenges** **Woon Leng Loh** Institute Of Microelectronics, Singapore	**G-02** Location: **Leo 1** **P243 - Challenges and Approaches of 2.5D high density Flip chip interconnect on**	**G-03** Location: **Leo 2** **P314 - Electrostatically induced voltages generated in ungrounded metal box and on the box when charged body**	**G-04** Location: **Leo 3** **P193 - Dual-band differential outputs CMOS Low Noise Amplifier** **Atsuhiro Hamasawa, Haruichi Kanaya** KyushuUniversity/Japan, Japan	**G-05** Location: **Leo 4** **P165 - Active Device Performance after Fan-out Wafer-level Packaging Process** **Hongyu Li, Masaya Kawano, Simon Lim, Daniel Ismael Cereno,**

		through mold interposer **Sharon Pei Siang Lim, Ser Choong Chong, Wenwei Seit, Tai Chong Chai** IME, Singapore	**moves away from the box** **Norimitsu Ichikawa** Kogakuin University, Japan		**Vasarla Nagendra Sekhar** IME, Singapore
	G-06 Location: **Gemini 2** **P210 - Within Die Coplanarity Improvement Strategies for Electroplated Cu Pillars** **Gabe Graham, Lee Peng Chua, Bryan Buckalew, Thomas Ponnuswamy, Steve Mayer** Lam Research, United States of America	**G-07** Location: **Leo 1** **P184 - High Density metal alloy Interconnections Using Novel Wafer Bonding Approach For 3D IC Packaging Applications** **Hemanth Kumar Cheemalamarri, Satish Bonam, Siva Rama Krishna Vanjari, Shiv Govind Singh** Indian Institute of Technology Hyderabad, India	**G-08** Location: **Leo 2** **P169 - Evaluation of Thermal Crack Propagation in Die-attached Joints Due to Cyclic Energization by Synchrotron Radiation Laminography Monitoring** **Junya Ooi[1], Toshihiko Sayama[2], Hiroyuki Tsuritani[2], Yoshiyuki Okamoto[3], Masato Hoshino[4], Kentaro Uesugi[4], Takao Mori[1]** 1: Department of Mechanical System Engineering, Toyama Prefectural University, Japan; 2: Machinery & Electronics Research Institute, Toyama Industrial Technology Development Center, Japan; 3: Design Engineering Department, Cosel Co., Ltd., Japan; 4: SPring-8, Japan Synchrotron Radiation Research Institute (JASRI)	**G-09** Location: **Leo 3** **P330 - Development of Deployable Catheter for Minimally Invasive Surgery Guidewire Application** **Weiguo Chen, Ramona Ramona, Ruiqi Lim, David Choong, Ming-Yuan Cheng** Institute of Microelectronics (IME), Singapore	**G-10** Location: **Leo 4** **P139 - Temporary Bonding Material Study for Room Temperature Mechanical Debonding with eWLB Wafer Application** **Seiya Masuda[1], Yu Iwai[1], Mitsuru Sawano[1], Kotaro Okabe[1], Kazuto Shimada[1], Joal Caparas[2], Won Kyoung Choi[2]** 1: FUJIFILM Corporation, Japan; 2: STATS ChipPAC Ltd, Singapore
	G-11 Location: **Gemini 2** **P222 - Hybrid Cu-SiN and Cu-SiOx Direct Bonding of 200 MM CMOS Wafers With Five Metal Levels: Morphological, Electrical and Reliability Characterization** **Celso Cavaco, Konstantinos**	**G-12** Location: **Leo 1** **P351 - Design and Modeling of Novel TSVs for Ternary Logic Applications** **Ramesh Vobulapuram[1], Durga Prasad[1], Ramana Reddy[1], Divya Madhuri Badugu[2]**	**G-13** Location: **Leo 2** **P267 - Effect of the laser parameters, epoxy mold compound properties and mold tool surface finishing on mark legibility of encapsulated IC package**	**G-14** Location: **Leo 3** **P303 - High Performance Package-Level EMI shielding of Ag Epoxy Composites with Spray method for High Frequency FCBGA package Application** **Kisu Joo, Kyu Jae Lee, Jung Woo Hwang, Jin-**	**G-15** Location: **Leo 4** **P347 - Development of Antenna in FO-WLP** **Serine Soh, David Ho, Hsiang Yao Hsiao, Simon Lim, Sharon Lim, Ser Choong Chong, Tai Chong Chai** Institute of Microelectronics, Singapore

	Chatzinis, Bert van Lijnschoten, Stefano Guerrieri Imec, Belgium	1: Rajeev Gandhi Memorial College of Engineering and Technology, India; 2: KL Deemed to be University	**Ming Siong Lim, Yuan Tat Chai** Infineon Technologies, Malaysia	**Ho Yoon, Yoon-Hyun Kim, Se Young Jeong** Ntrium Inc., Korea, Republic of (South Korea)	
	G-16 Location: **Gemini 2** **P346 - Development of FO-WLP Package-on-Package using RDL-first Integration Flow** **Soon Wee Ho, Hsiang-Yao Hsiao, Siak Boon Lim, Leong Ching Wai, Ser Choong Chong, Pei Siang Lim, Tai Chong Chai** Institute of Microelectronics, Singapore	**G-17** Location: **Leo 1** **P263 - Enabling Flip Chip QFN Technology: Understanding Kirkendall Voiding and Factors Affecting its Formation during Bumping Process** **Ruby Ann Dizon Mamangun, Rafael Jose Lizares Guevara, Jose Arvin Matute Plomantes** Texas Instruments Philippines, Inc., Philippines	**G-18** Location: **Leo 2** **P315 - An Alternative Packaging Solution in Achieving Moisture Sensitivity Level One (1) for Small Outline Integrated Circuit (SOIC) Automotive Packages** **Alvin Denoyo, Rod Delos Santos Jr., Darwin De Lazo, Ivan Gil Costa, Allen Menor** ON Semiconductor, Philippines	**G-19** Location: **Leo 3** **P150 - Design and optimization of the 10Tbps optical transmission system** **Huimin He[1,2], Fengman Liu[1,2], Haiyun Xue[1,2], Yu Sun[1,2], Liqiang Cao[1,2]** 1: Institute of Microelectronics of Chinese Academy of Sciences; 2: National Center for Advanced Packaging Co.LTD	**G-20** Location: **Leo 4** **P154 - Study of the die potion accuracy in the fabrication process of a die first type FO-PLP** **Keisuke Nishido, Hitoshi Onozeki, Naoya Suzuki, Toshihisa Nonaka** Hitachi Chemical Co.,Ltd., Japan
3:20pm - 3:40pm	**Tea/Coffee Breaks-06: Interactive Session 2** Location: **Pisces**				
3:40pm - 5:40pm	**Plenary Session 3: Next Generation Packaging Technologies** Location: **Virgo** Mr. Shigenori Aoki, Fujitsu Laboratories (Moderator) 1. Yasumitsu Orii, NAGASE "Packaging Technologies for Brain-inspired Devices in the era of AI/IoT" 2. Yasushi Masuda, Fujitsu Advanced Technologies "Challenges and opportunities of packaging technologies for next generation computer systems" 3. Hideyuki Nasu, Furukawa Electric"VCSEL-based Optical Interconnects" 4. Toshihisa Nonaka, Hitachi Chemical "Material technology can drive advanced packaging"				
5:40pm - 6:00pm	**Closing Ceremony: Lucky Draw** Location: **Virgo**				

Date: Thursday, 06/Dec/2018

10:00am - 11:00am & 3.40pm - 4.40pm	**Interactive Session 1** Location: **Pisces** **P104 - Kirkendall Voids Improvement in Thin Small No Lead Package** **Lay Yeap Lim, Yau Huang Huang** Infineon Technologies Sdn Bhd, Malaysia **P105 - Characterization of interfacial intermetallic compounds in gold wire bonding with copper pad** **Bisheng Wang[1], Lois JinZhi Liao[2], Xiaomin Li[2], Younan Hua[2], Chao Fu[2]** 1: Huawei Technologies Co Ltd; 2: WinTech Nano-Technology Services Pte. Ltd **P114 - Failure Analysis on Mobile Phone Batteries and Accessories** **ZHI JIN[1], HIroshi NISHIKAWA[1], Y.C Chan[2]**

1: Osaka Univerisity, Japan; 2: City University of Hong Kong, China

P117 - High modulus DAF Introduction to decrease thin die WB crack issue

Ling Yang, Allen Ji
Sandisk/Western Digital, China, People's Republic of

P120 - Effect of electric current on constitutive behaviour and microstructure of SAC305 solder joint

Wenbin Tang[1], Xu Long[1], Yongchao Liu[2], Chongyang Du[1], Yao Yao[1], Cheng Zhou[3], Peiyan Wu[3], Fengrui Jia[4]
1: School of Mechanics, Civil Engineering and Architecture, Northwestern Polytechnical University, Xi'an, China; 2: College of Mining Engineering, Liaoning Shihua University, Fushun, China; 3: Space Research Institute of Electronics and Information Technology, Aerospace Science and Technology Corporation, Xi'an, China; 4: College of Petroleum Engineering, Liaoning Shihua University, Fushun, China

P125 - Void Defect Formed in Wiping Step of Gravure Printing

Zhanhong Cen, Xuechuan Shan, Budiman Salam, Lee Siew Rachel Tan, Jun Wei
Singapore Institute of Manufacturing Technology, Singapore

P130 - Research on Feedforward Control in the linear motor direct drive XY two-dimensional platform

Yunbo He, Zuoxiong He
Key Laboratory of Precision Microelectronic Manufacturing Technology & Equipment of Ministry of Education, School of Electromechanical Engineering, Guangdong University of Technology, Guangzhou, P.R.China

P132 - Development of Thermal Test Package for Data Center Micro-Fluid Cooling Characterization

Yong Han, Boon Long Lau, Gongyue Tang, Sharon Seow Huang Lim, Xiaowu Zhang
Institute of Microelectronics, A*STAR, Singapore

P136 - RSSDs Thickness Impact on Storage System and Assessment by Pseudo Curve

Feng Qi, Casey Winkle, Xudong Tang
Intel

P138 - How my electronics is influenced by housing: A Thermal Point of View Study to Understand the Impact of Housing on Internal Air Temperature

Nitesh Kumar Sardana, Kratika Shrivastava
Robert Bosch Engineering and Business Solution Pvt Ltd, India

P143 - Study of polysilsesquioxane dielectric for the use of multi-structured redistribution layers in fan-out wafer level packaging applications

Changmin Song, Sungdong Kim, Sarah Eunkyung Kim*
Seoul National University of Science and Technology, Korea, Republic of (South Korea)

P144 - High Aspect Ratio~10 TSV Via-last-from-back Process Development and Integration

Xiangyu wang, Hongyu Li
Institute of Microelectronics (IME), A*STAR (Agency for Science, Technology and Research), Singapore

P146 - Joint Feature Automatic Classification for Aluminum Wire Bonding Based on KPCA and Random Forest

zhili long, xing zhou, xiaobing zhang, ronghua he
Harbin Institute of Technology Shenzhen Graduate School, China, People's Republic of

P147 - Effect of Ar-N2 Plasma Treatment on Copper Surface for Cu-Cu Wafer Bonding

Hae=Sung Park, Sarah Eunkyung Kim*
Seoul National University of Science and Technology, Korea, Republic of (South Korea)

P152 - Numerical Investigation on the Condensation Heat Transfer of FC72 in the Presence of Air

Pengfei Liu, Huicheng Feng, Kandasamy Ranjith, Teck Neng Wong, Kok Chuan Toh
Nanyang Technological University, Singapore

P155 - Study on bottom-up Cu filling process for Through Silicon Via (TSV) metallization

Gilho Hwang, Hsiang-Yao Hsiao, David Soon Wee Ho
Institute of Microelectronics, Singapore

P156 - Analysis of Low Profile Ferrite Material Based Planar Shell Core Inductor

Zeeshan Umar[1], Maciej Wojnowsk[1], Franz Xaver Engelsberger[1], Amelie Hagelaue[2], Robert Weigel[2]
1: Infineon Technologies, Germany; 2: University Erlangen-Nuremberg

P158 - Coated Silver Wire Bond: Reliability of Epoxy Molded Device

Murali Sarangapani, Senthilkumar Balasubramanian, Eric Tan Swee Seng, Jason Wong Chin Yeung
Heraeus Materials Singapore Pte Ltd, Singapore

P162 - Impact of lifetime and mechanical behaviors on TIM performance on high-end processor

Gamal Refai-Ahmed, Ho Hyung Lee, Hoa Do
Xilinx, United States of America

P166 - Mm-Wave Antenna in Package (AiP) Using Unbalanced Substrate with and without Solder Mask.

Kuan-Ta Chen[1], Bo-Siang Fang[2], Ying-Wei Lu[3], Chia-Chu Lai[4]
1: SPIL, Taiwan; 2: SPIL, Taiwan; 3: SPIL, Taiwan; 4: SPIL, Taiwan

P178 - Discussion of the Signal Transmission Crosstalk

Yi Ting Tsou, I Huai Wang, Sung-Mao Wu
National University of Kaohsiung, Taiwan

P186 - Correlating Printing Performance of Solder Paste with Its Rheology

Saurabh Shrivastava, Ansuman Das, Sathiyanarayanan C
Alpha Assembly Solutions, A Macdermid Performance Solutions Business, India

P191 - Laser hybrid integration on silicon photonic integrated circuits with reflected grating

Yu Sun[1,2], Man Zhao[1,2], Juan Wei[1,2], Fengman Liu[1,2], Haiyun Xue[1,2], Huimin He[1,2], Liqiang Cao[1,2]
1: Institute of Microelectronics of Chinese Academy of Science,, China, People's Republic of; 2: National Center for Advanced Packaging Co.,LTD (NCAP China), China,People's Republic of

P197 - Block-Based Finite Element Modeling, Simulation and Optimization of the Warpage of Embedded Trace Substrate

Chien-Yu Lien, Yao-Chen Chuang, Yuan Yao
National Tsing Hua University

P201 - The Balun Design by Embedding High Permittivity Material in The Substrate of CSP Package with Large Size

Ying-Wei Lu, Bo-Siang Fang, Hsuan-Hao Mi, Kuan-Ta Chen, Mike Tsai
Siliconware Precision Industries Co., Ltd., Taiwan

P220 - Evaluating moldability challenges in a Large Strip Package with Transfer Molding Process simulation

Subramanian N.R.
Infineon Technologies Asia Pacific Pte Ltd, Singapore

P223 - Electrokinetic Behavior of Solder Powders in Non-aqueous Media

	Terence Lucero Fernandez Menor, Manolo G. Mena, Herman D. Mendoza University of the Philippines, Diliman **P226 - Effect of Bond Pad Surface Finish on AuSn Solder Bumping Using Laser Solder Jetting** **Norhanani Jaafar, Chong Ser Choong** Institute of Microelectronics, Singapore

Date: Friday, 07/Dec/2018

10:20am - 11:10am & 3.20pm - 3.40pm

Interactive Session 2
Location: **Pisces**

P231 - A New Failure Mechanism of Inter Layer Dielectric Crack
Haiyan Liu, Xiangyang Li, Jun Li, Sean Xu
NXP, China, People's Republic of

P233 - Package Level Warpage Simulation of Fan-Out Wafer Level Package Considering Visco-Elastic Material Properties
ZHAOHUI CHEN
IME A-Star, Singapore, Singapore

P236 - Solution for Short Tail Issue on Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG) Bond Finger with 0.7mil Gold Wire
Leong Ching Wai, Teck Guan Lim
Institute of Microelectronics, Singapore

P259 - Study on Ultra-thin & High-Pixel CMOS Image Sensor Module
Mark Huang, Huisheng Han, Huabin Wu, Chuangwen Huang, Weiqing Zhang
A-Kelon (Huizhou) Optronics Ltd., China, People's Republic of

P264 - Millimeter-wave resonator and cavity-back slot antenna in Fan-Out Wafer Level Packaging
Zihao Chen, Teck Guan Lim
Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research)

P265 - Film Type PID Material
Toshizumi Yoshino, Toshimasa Nagoshi, Shuji Nomoto, Akihiro Nakamura
Hitachi Chemical, Japan

P273 - fine pitch solder paste for advance packaging application
ruifen zhang
heraeus material singapore, Singapore

P279 - A Complete Explanation of Warpage Behavior Across Backend Processes on Organic BGA in Strip Form and its Predictive Methodology
Jing-en Luan, Roseanne Duca
STMicroelectronics Pte Ltd, Singapore

P286 - Characterization and Performance of Ultrafine Lead-Free powders
Wei Chih Pan[1], Leng Hin Tan[1], Yee Ting Lo[1], Li San Chan[1], Sebastian Fritzsche[2]
1: Heraeus Materials Singapore, Singapore; 2: Heraeus Deutschland GmbH & Co. KG

P287 - Mechanics of Copper Wire Bond Failure due to Thermal Fatigue
Stevan G Hunter[1,2], Subramani Manoharan[2], Patrick McCluskey[2]
1: ON Semiconductor, United States of America; 2: University of Maryland

P289 - Integration of Tungsten micro-heaters and polymer microfluidic for the cell sorting application.

Bivragh Majeed, Lut Van Acker, Koen De Wijs, Chengxun Liu
imec, Belgium

P290 - Surface planarization of polymeric interlayer dielectrics for FOWLP applications

Soojung Kang, Yejin Kim, Ayoung Moon, Sangwon Lee, Sarah Eunkyung Kim, Sungdong KIM
Seoul National University of Science and Technology, Korea, Republic of (South Korea)

P296 - Investigation of solder void and packages crack defect in flip chip packaging by 3D computed tomography analysis.

Chin Yung Lai
Infineon, Malaysia

P299 - Microstructure of Press-fit Connection and Its Impact on Board Level Reliability

Aruna Palaniappan[1], Li Li[2], Tae-Kyu Lee[1]
1: Portland State University, United States of America; 2: Cisco Systems, United States of America

P308 - Improvement of die shift by solder self-alignment for fan-out package process applications

Hwanpil Park, Sungchul Kim, Jae-Yong Park, Young-Ho Kim
Hanyang University, Korea, Republic of (South Korea)

P313 - A Modified Unequal Wilkinson Power Divider Using T-Shaped Transformers

Ren-Fu Tsai[1], Pu-Hua Deng[2], Ting-Jung Chang[3]
1: Department of Electrical Engineering, National University of Kaohsiung; 2: Department of Electrical Engineering, National University of Kaohsiung; 3: Department of Electrical Engineering, National University of Kaohsiung

P317 - RDL Process Development of MEMS Wafer Level Chip Scale Packaging with Silicon Pillar/CuPd as Through Mold Interconnection

Boon Long Lau[1], Zhaohui Chen[2], Siak Boon Lim[3], Pei Siang Lim[4]
1: IME astar, Singapore; 2: IME astar, Singapore; 3: IME astar, Singapore; 4: IME astar, Singapore

P320 - Power Integrity Analysis for Active Silicon Interposer

Zihao Chen[1], Teck Guan Lim[2]
1: IME,A*STAR, Singapore; 2: IME,A*STAR, Singapore

P321 - Characterization of PECVD of Amorphous Silicon Films from 150°C to 400°C

HOU JANG LEE
Institute of Microelectronics, Singapore

P325 - Robust Packaging For MEMS Sensors Using Plastic Moulding

Guoqiang Wu, Leong Ching Wai, Daw Don Cheam, Peter Hyun Kee Chang, Navab Singh, Yuandong Gu
Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore

P337 - Face-up Interconnection Technique Using Direct Image Writing for Three-Dimensional Heterogeneous Flexible Electronics

Houngkyung Kim, Yongjin Kim, Jun Yeob Song, Jae Hak Lee, Seungman Kim
Korea Institute of Machinery & Meterials, Korea, Republic of (South Korea)

P339 - Demonstration of Ultra-fine Pitch Au-Au Diffusion Bonding on Chip-on-Film (COF) with IGEPIG Surface Finishing

Pun Kelvin[1], Rotanson Jason[1], Chan Alan H.S[2]
1: Compass Technology Co Ltd, Hong Kong S.A.R. (China); 2: City University of Hong Kong

P344 - Effect of wire bonding on the performance of RFMEMS filters

Nan Wang, Yao Zhu, Teck Guan Lim, Navab Singh, Yuandong Gu
Institute of Microelectronics, Singapore

P345 - A Lame Mode Resonator Based on Aluminum Nitride on Silicon Platform

Nan Wang, Yao Zhu, Guoqiang Wu, Zhipeng Ding, Eldwin Jiaqiang Ng, Nishida Yoshio, Peter Hyun Kee Chang, Navab Singh, Yuandong Gu
Institute of Microelectronics, Singapore

P352 - A Novel Shielding Technique to Reduce the Crosstalk Effects in TSVs

Divya Madhuri, Sunitha Mani
KL University, India

P356 - Laser Drilling of Thru Mold Vias for FOWLP Application

Vasarla Nagendra Sekhar, David Soon Wee Ho, Srinivasa Rao Vempati, Ismael Cereno Daniel
Institute of Microelectronics, Singapore

P359 - A hybrid laser integration approach for miniature photonics sensors

JIFANG TAO, Ser Choong Chong, Tao Sun, Hong Cai, Navab Singh, Yuandong Gu
Institute of Microelectronics, Singapore

P360 - Solder Sphere Transfer for wafer level Packaging

Florian Bieck, Robert Thalmann, Christoph Glaubitz, Tom Friedrichson
PacTech Asia, Malaysia