"Emerging NAND Memory Packaging Challenges"

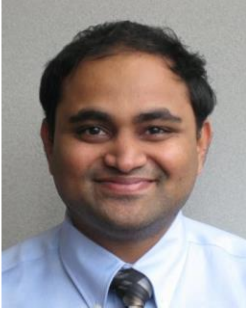
Dr. Gokul Kumar is a Principal Engineer with the Packaging & Assembly Group at Western Digital, Milpitas, USA.

NAND Flash is the primary storage of choice for smart phones, tablets and solid-state drives. The electrical requirements for this memory has exponentially evolved from its original multimedia consumer applications (with uSD cards, USB, audio players, cameras, cell phones) into enterprise storage and server farms. In this latter space, it has become an indispensable component in the memory hierarchy of large storage systems. Penetration into these markets is fueled through a relentless improvement in cost per bit by two factors: a) Migration to 3-D monolithic NAND fabrication process and b) Aggressively growing the number of dies stacked using advanced packaging techniques, from 1 die in 2003 to 16 dice in 2014.

A roadmap based on 3-D monolithic NAND process has created situation where the ability to predict technology behavior is no longer solely based on scaling lithography. Rather, each node is connected to a combination of parameters such as cell diameter, vertical cell pitch, numbers of cells in a stack and the number of bits per cell. While both these factors independently cause well-established packaging challenges, their intertwined interactions have resulted in addition considerations.

Stacking more memory dice within a given package height or to reduce package thickness continues to reduce individual die thickness. Such thinner die has lower rigidity, larger warpage, and poorer strength. The arising challenges from thin die assembly and device reliability of extremely thin NAND memory dies have been discussed based on our experimental and simulation studies. Modeling methods to predict arising warpage arising from corresponding substrate thinning has also been published. This paper presents an overview of critical challenges from a) materials, b) process, and c) design of NAND packages and proposes solutions based on experimental and analytical studies.

In this work, the first section examines critical processing challenges due to thin die stacking. The process of mechanical saw spin dicing on the very thin flash creates chip out (particles), micro-cracks start to propagate and impact active circuit zone. This paper explores tighter thickness tolerances on back-grinding equipment, including optical dicing methods. The use of high modules DAF materials to prevent cracking from thin-die at overhang locations as a part of the die stack is also studied. A combination of more than 4 different categories of materials is used in semiconductor packages, including semiconductor material, metals, organic polymer and dielectric materials. The subsequent section analyzes the warpage challenges specific to NAND stacking die and substrate materials. The EMC compound selection and improvement opportunities to enable overall thin packages is analyzed. The final section examines design challenge arising from the technical point of view on substrate design and integration of ASIC flip-chip dies along with NAND memories. In addition, additional unknowns in NAND 3-D integration using TSVs present from both cost and technology perspective are discussed.



Dr. Gokul Kumar is a Principal Engineer with the Packaging & Assembly Group at Western Digital, Milpitas, USA. He has a multi-disciplinary expertise in the areas of packaging of electronic systems, signal and power integrity, 3-D integration. Previously, he worked on developing 3-D interposers within the glass/silicon interposer consortia at the 3-D packaging research center in Georgia Tech. He has coauthored about 15 conference and journal publications, with 1 issue patent and 5 others pending. He regularly reviews papers for IEEE CPMT, and several other conferences including EPEPS, International Midwest Symposium on Circuits and Systems, etc.

He received his PhD and MS specializing in Electrical and Computer Engineering, from the Georgia Institute of Technology in 2015 and 2010 respectively.

"Electronic Materials and Packaging Trends in the Era of Digital Transformation"

Rozalia Beica, Global Director Strategic Marketing, Electronics & Imaging, Specialty Products Division of DowDuPont

Digital transformation is further expanding into new markets bringing new application opportunities and driving increased adoption of electronics and semiconductor devices. The explosion of new applications is driving the semiconductor industry to transition from a technology node to an application driven industry. While advancing the technology node continues, new architectures and integration technologies are being developed to address the increased market requirements and the need of integrating more functionalities within smaller and more compact systems. A wide range of packaging technologies have already been successfully developed and adopted in the industry enabling single and multi-die packaging. While these technologies will continue to grow and further evolve, heterogeneous integration is gaining a lot of interest in the industry due to several benefits it can bring. This will also drive the need for more performing electronic materials and processes.

The presentation will provide an overview of the major trends (5G, Artificial Intelligence, IoT, Autonomous Driving, etc.) driving the semiconductor and packaging industry. The talk will highlight the various packaging platforms and their evolution as well as the material and processing challenges and needs driven by the new applications. Examples of DowDuPont activities and materials and its commitment to future innovation, collaboration and sustainability will also be included.

Rozalia Beica, Global Director Strategic Marketing, Electronics & Imaging, Specialty Products Division of DowDuPont.

In her current role, Rozalia leads strategic marketing activities across Electronics & Imaging Division. She has 25 years of international working experience across various industries, including industrial, electronics and semiconductors. For 19 years she was involved in the research, applications and strategic marketing of Advanced Packaging technologies, with global leading responsibilities at specialty chemicals (Rohm and Haas Electronic Materials), equipment (Semitool, Applied Materials and Lam Research) and device manufacturing (Maxim IC). Prior to joining Dow, Rozalia was the CTO of Yole Développement where she led the market research, technology and strategy consulting activities for Advanced Packaging and Semiconductor Manufacturing.

Throughout her career, Rozalia has been actively supporting industry activities worldwide: Program Director of EMC3D Consortia, General Chair of IMAPS Device Packaging and Global Semiconductor and Electronics Forums, Technical Advisory Board Member at SRC, Member of the Executive Committee of ECTC, IMAPS SiP, ISQED, ESTC and member of several committees worldwide (ITRS, IWLPC, EPTC and EPS). Current industry

involvements include: IMAPS VP of Technology, Technical Chair IMAPS Advanced SiP, Executive Committee Member of SiP China, ECTC Assistant Program Chair, HIR WLP Chair, Advisory Board Member of 3DinCites and IMPACT Taiwan. She has over 150 presentations and publications (including 3 book chapters on 3D IC technologies), several keynotes, invited presentations and panel participations.

Rozalia has a M.Sc. in Chemical Engineering from Polytechnic University "Traian Vuia" (Romania), a M.Sc. in Management of Technology from KW University (USA), and a Global Executive MBA from Instituto de Empresa Business School (Spain).

"Submicron Polymer Re-distribution Layer Technology for Advanced InFO Packaging"

Dr. Han-Ping Pu, Deputy Director of Advanced Packaging Division in TSMC R&D, Hsinchu, Taiwan

High-performance computing (HPC) applications such as Artificial Intelligence (A.I.) have been the hot topic in recent years. The advanced multi-chip packaging plays an important role for fast time-to-market and cost effective solution instead of SOC. For the increasing bandwidth requirement, more I/O die to die communications for advanced packaging is a need. To fulfill this demand, large number in registered routing lines between dies lead a constant drive for miniaturization for die to die Redistributed Layer (RDL) among industry. To achieve this, it is undoubtedly to induce the demand of dimensional scalability on line-width and corresponding via size of die-to-die interconnects, to be deployed for providing more communications between chips.

In this talk, InFO Ultra-High-Density (UHD) RDL technology is presented for die-to-die communication with RDL line-width down to submicron range (<1um) [1, 2]. It is preferable to be designed to manufacture from packaging-industry available tool sets instead of Cu/low-k in BEOL counterpart, to ensure competitiveness in cost to other techniques in current commercial market. Accordingly, for this technology, Cu RDL and Cu via are deployed by PVD barrier/seed with following electro-plating process, plus sufficient process support from etching, ash, and lithography to realize the designed fine line dimensional architecture consisted of two RDL layers at least. All tool sets have been intentionally and initially arranged from current commercialized industrial packaging available processing and metrological tools with necessary retrofit, for both purposes of cost consideration and process adopted availability.

The InFO UHD RDL technology is characterized by electrical performances, e.g., via-chain continuity, RDL Comb/Meander Rs, line-to-line leakage current, and eventually interconnect reliability testing such as electro-migration (EM), stress migration (SM), breakdown voltage (Vbd), Time-Dependent-Dielectric Breakdown (TDDB), etc. After process optimization, the electrical test data demonstrate >99% yields from via-chain continuity, RDL Comb/Meander Rs and leakage current. Initial interconnect reliability testing shows good performance from EM, SM, Vbd, TDDB, etc. Our UHD line and via EM performances are compatible to commercial L/S 2/2um, 5/5um, and 10/10um RDL EM performances. SM results pass TSMC internal criteria for UHD technology under via SM of Via 1.5um, and also for the case of both line/via SM in the L/S 1/1um with Via 2um. For Vbd and TDDB, we conduct the wafer-level testing under relatively severe conditions, as Vbd at 125oC with ramping stressed voltage rate of 1V/0.5 sec from 0 to 100 volts, and TDDB at constant 200 volts at 125oC. Even under these conditions, both Vbd and TDDB data still pass without failure. For InFO level reliability test, the torturing condition is employed as MR (Multiple Reflow) before deploying

electrical properties measurement. It is evident that all MR samples pass the criteria without any failure. Furthermore, we conducted TCB 700 cycles (-55oC to 125oC thermal cycling condition) and recognize no failure occurred as well.
Heading to miniaturization furthermore of RDL dimension in the future for various applications and benefits of more inter-chip communication paths, possible materials change, for instances of RDL dielectric materials, molding materials, and lithographic photoresist materials, etc., would definitely be included in any look-ahead plan. Low-temperature process based dielectric materials would be popular to fulfill flexibility in various applications of inter-chip connections, such as logic to memory die combination in one package. Meanwhile, for any new approaches including both materials change and innovative integration flow proposals, simulation always provides a handy methodology for us to determine strategically any possibility beforehand. Additionally, both process and metrological tools of current phase might need to be retrofitted or even be re-developed. Furthermore, any approach to enhance line or via strength, or to boost EM/SM performances are definitely welcome. Many similar examples can be seen or predicted, and we might even face some unknown challenges as miniaturization technology evolution continues in the future.

Han-Ping Pu received Ph.D. degree in Materials Science and Engineering from National Sun Yat-Sen University, Kaohsiung, Taiwan, in 1995. He devoted himself to the field of semiconductor packaging for over 20 years. His career is mainly focus on advanced packaging development, package modeling and resolving chip-package interaction issues. He is now a Deputy Director of Advanced Packaging Division in TSMC R&D, Hsinchu, Taiwan. He has been involved in the invention of over 80 US patents and published more than 10 technical papers in semiconductor packaging area. He is an IEEE and EPS member.

“Temporary Wafer Bonding Technology for Advanced Packaging”
Dr. Dongshun Bai, Deputy Business Development Director of the Wafer-Level Packaging Materials business unit at Brewer Science.

The current drivers for the semiconductor industry are consumer electronics, mobile devices, cloud computing, automotive electronics, 5G technology, and Artificial Intelligence. While the semiconductor industry continues to make progress in scaling integrated circuits, it is also turning to advanced packaging technologies to increase performance and integration while lowering costs. The advanced packaging landscape is changing at an astonishing

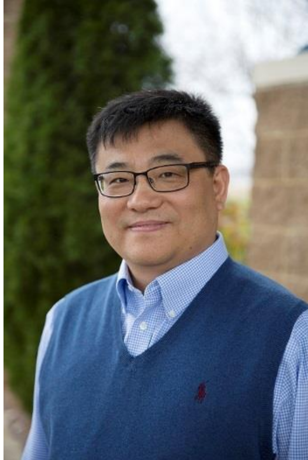
speed, and the demand for faster, smaller, lower-cost devices with reduced power consumption is now greater than ever.

Brewer Science was one of the first companies to consider temporary wafer bonding as an enabling technology for ultrathin wafer handling. More than ten years ago, we recognized that thin substrate handling is a fundamental processing need that cuts across many forms of advanced packaging. Nowadays, temporary bonding is not only used for wafer thinning and backside wafer processing at high temperatures and high vacuum levels, but also enables the handling of new types of packaging substrates such as reconstituted wafers and panels that easily deform under thermal stress.

To satisfy the wide range of processing requirements for different substrate types, more features must be considered in the design of temporary bonding materials. It is impractical, if not impossible, to cover the entire range of market needs with one material set or type. We have adopted a portfolio approach to material development and we utilize many different platforms to address the needs of this fast-paced market. After over 10 years of development, we have an extensive portfolio of temporary bonding materials that are compatible with all common modes of debonding, including chemical, slide, mechanical, and laser release. We are also developing new materials such as permanent adhesives, laser ablative dielectrics, and others for leading-edge packaging applications.

The presentation will illustrate the requirement and challenges for the carrier-assist substrate handling technology and introduce the advancements in the area of materials and processes that enable advanced packaging schemes such as fan-out packaging, system in package, and 3D/2.5D technology technologies. A novel dual-layer platform will also be introduced. The dual-layer system was developed to aid thin wafer handling (TWH) processes within multiple market segments including: III-V compound semi, power, 3DIC, memory, eWLB, MEMS and other FOWLP segments – all of which have stringent requirements with respect to adhesion, low total thickness variation (TTV), temperature stability, performance and form factor.

The dual-layer platform includes two layers: a thermoplastic layer and a curable layer that can be either UV- or thermally cured depending on the application. The thermoplastic layer is a conformal adhesive layer applied to the device that protects the device structures. This soluble thermoplastic layer has high glass transition temperature (Tg) and little to no melt flow at high temperature. The curable layer is applied on the carrier. It exhibits high melt flow prior to curing to enable low-temperature bonding and no melt flow after curing. Together, the two layers, which do not intermix or react chemically, enable mechanical stability and provide thermal stability up to 400°C. This system can be used with either mechanical or laser debonding methods. Other advantages of the dual-layer system include increased throughput and easy to clean after processing.

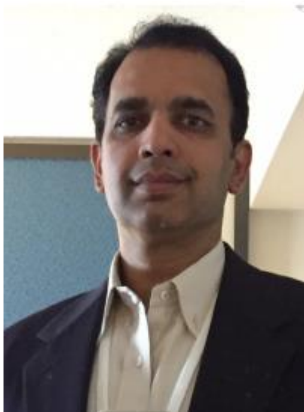


Dongshun Bai earned his Ph.D. in Chemical Engineering from Vanderbilt University. In 2007, he joined Brewer Science, Inc., where he has worked as Senior Scientist and Senior Program Manager in the Advanced Technologies R&D group and led the R&D work on temporary bonding and release materials. He is currently the Deputy Business Development Director of the Wafer-Level Packaging Materials business unit at Brewer Science.

"A Framework for Reliability Assessment of Chemical-Induced Display Delamination"
Dr. Kedar Hardikar, Module Reliability Engineering Lead (Mechanical) in Google's Consumer Hardware division.

Touch-enabled displays in handheld and wearable devices are expected to meet aggressive design requirements in harsh use conditions. The use conditions include exposure to household chemicals like sweat, hand lotion, sunscreen in addition to high temperature and high humidity conditions. Typical applications include smart phones, smart watches, touch bar of a MacBook Pro, and tablet PCs. This study examines chemical induced interfacial delamination within a display module. A typical display stack up consists of cover glass, optically clear adhesive, polarizer, touch panel, pressure sensitive adhesive, poly-imide based pOLED, PET film, and conductive adhesives. The lamination process, which varies from one display manufacturer to the other, typically leaves the display stack in a state of internal stress. Other than the cover glass, the edges of the display stack are susceptible to degradation due to exposure to chemicals.
Conventional approach to address the degradation risk is to develop product design constraints (example: enclosure) that provide sufficient resistance to ingress of chemicals and moisture. However, Industrial Design requirements of lighter weight and slimmer form factors may prevent successful protection of the edge of the display stack. Hence, characterization of chemical induced delamination failures is critical for display reliability assessment. In this work experiments are conducted with the display edge exposed to specific chemicals. This is considered to be a limiting case of chemical exposure for display module edge. It is observed that in this test the delamination is typically initiated at a point along the edge and proceeds as an approximate semi-elliptical crack front. It is further observed that the growth rate of the crack front diminishes exponentially with time, and
the crack attains a limiting dimension. Furthermore, accelerated testing carried out at elevated temperature and humidity conditions shows that the crack growth has the same

exponential behavior. The observed delamination can be modeled as a semi-elliptical interfacial crack front. If such delamination is driven primarily by internal stresses the energy release rate for the delamination decreases as the delamination
size increases and hence such delamination would be self-limiting where the limiting size is a function of the magnitude of internal stresses and the conditions to which the display stack is subjected in the test. This is consistent with the observed delamination failures.
The observed delamination induced in this test can be modeled as a semi-elliptical interfacial crack front. Based on classical fracture mechanics, crack growth occurs when strain energy released during crack growth exceeds the energy required for the creation of the new fracture surface. The semi-elliptical crack front suggests that the crack growth is driven by stresses that are almost isotropic. High magnification photos of the crack front show the dendritic features typical of internal stress driven delamination. Hence, internal stresses within the display stack up, induced by the lamination process, is considered to be the primary driver of this interfacial crack. Creation of a new fracture surface (crack growth) relieves the internal stresses in the display stack, thus decreasing the incremental energy available for creation of new surfaces. This reduces the crack growth rate in
an asymptotic manner till it reaches it limiting dimension.
While fracture energy considerations can be used to understand the self-limiting nature of such delamination, temporal evolution of such defects is not easily amenable to analysis. Since a theoretical analysis is beyond the scope of this paper, an empirical equation is proposed to describe the evolution of interfacial delamination with time. The proposed relation is shown to describe the experimental data satisfactorily. Such quantification of the time-evolution of delamination enables evaluation of different display stacks in a structured manner. Finally, it is shown that this characterization framework can enable an enhanced reliability assessment of the module reliability data.

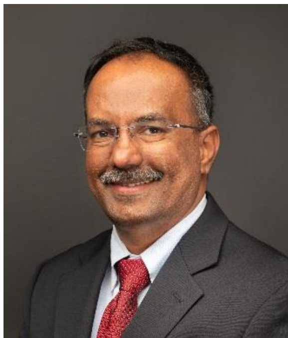


Dr. Kedar Hardikar is the Module Reliability Engineering Lead (Mechanical) for products developed by Google's Consumer Hardware division. In addition, he is an adjunct faculty member at San Jose State University,California.
He holds a Ph.D in Solid Mechanics from the Division of Engineering, Brown University, and has over 10 years of technical leadership experience in semiconductor capital equipment, solar, and consumer electronics industries.
Dr. Hardikar has authored several technical publications and offered invited talks, including an invited paper in JMPS and an invited talk at NIST. Before joining Google, he was the Director of the Reliability Integration Simulation and Certification (RISC) group at Miasole, a global leader in CIGS PV technology.

“Packaging for Performance Scaling”

Sam Karikalan, Senior Manager at Broadcom Inc., Irvine, California

Slowing down of Moore’s law has forced the industry to come up with innovative ways of scaling up semiconductor device performance with the help of heterogeneous integration packaging technologies. Process technologies for Substrates, Silicon Interposers, Through-Silicon-Vias and Fan-Out packaging that are needed for such high end packaging, are all slowly maturing towards high yields. However the Electrical, Thermal and Mechanical performance demand for these package types will keep growing steadily in the coming years, as the end use applications of these devices constantly push the envelope on speed and power. This talk would present the design challenges posed by such performance needs and discuss the areas that need to be jointly addressed by the design, materials and process engineering communities to be fully prepared.



Sam Karikalan is a Senior Manager at Broadcom Inc., Irvine, California, leading a global team of Signal Integrity, Thermal and Mechanical design experts that is responsible for package design optimization for performance in networking, broadband, storage, wireless and mobile devices. Sam has been with Broadcom for over 13 years. Prior to that, he worked for STATS ChipPAC, Primarion and Advanced Micro Devices on electrical modeling and characterization, package design optimization for electrical performance and component level EMI. The first ten years of Sam’s 31 yearlong industry experience was on System Level EMI/EMC at SAMEER-Centre for Electromagnetics in India, being responsible for EMC Compliance Testing, EMI fixes and EMC Design. Besides package design optimization for SI/Thermal/Mechanical performance, Sam is also currently working on Package Technology Development for Performance Scaling, such as 2.5D Integration, extensively working with the supply chain. He has 22 issued US patents and several papers in International Conferences/Journals to his credit. He is a Senior Member of the IEEE and a Member-at-Large on the Board of Governors of the IEEE Electronics Packaging Society. Sam also served as the General Chair of the 2018 IEEE Electronics Components and Technology Conference (ECTC), held in San Diego, California this year.

"ESD, EOS and AMR"

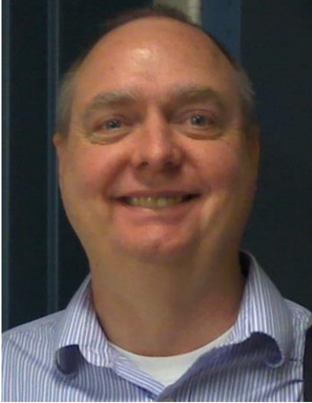
Dr. Stevan Hunter, Reliability Engineering Consultant and ESD Control Champion at ON Semiconductor in Phoenix, Arizona, USA

Semiconductor product and IC suppliers take great care to control static voltages and discharges, ESD, and any form of electrical overstress (EOS) during manufacture and shipping, in order to ensure that each part arrives to the customer with its full reliability. Yet a high percentage of customer returns claiming unreliability has electrically induced physical damage (EIPD), indicating that ESD or EOS events occurred after the parts were out of the supplier's hands. Increased awareness and control of ESD and EOS is needed in the whole electronics industry, not just with semiconductor suppliers.

ESD is actually just one category of electrical overstress (EOS). ESD is considered as an unpowered category of EOS. EOS damage that is not ESD can also be caused in powered handling such as "hot plugging" and "switching", whether the victim parts are single or in an assembly, module or system. Control of electrostatic discharge (ESD) events is important because semiconductor devices can be physically damaged, causing failure and yield loss for the supplier. Or worse, ESD damage could be "latent", not activating until some unpredictable time later, causing an "unreliability failure" for a customer. CMOS products are especially sensitive to electrostatic discharge, but actually any electronic part can be damaged if the ESD event is severe enough. Each semiconductor product is tested for ESD tolerance as part of the product qualification, with modern IC's typically being designed to withstand greater than 1000V. Semiconductor customers must be just as careful as suppliers in controlling ESD. Even when ESD-sensitive parts are already be attached to a board, damaging ESD discharges can still occur, such as Charged Board Event and Cable Discharge Event.

Semiconductor suppliers also carefully control voltage levels during testing, to prevent electrical overstress (EOS). This includes reliability stress testing. The supplier may actually test or stress parts for short times at voltages higher than the published operating voltage for their own purposes, including burn-in or other stresses that can reveal the presence of defects. Of course any parts with weaknesses detected are either repaired or scrapped. Certain product quality reliability stress tests include higher voltage and other stresses, to "accelerate" the weakest failure mechanisms. A successful product qualification indicates that those batches of parts from manufacturing are sufficiently reliable to perform for the full warranty period. Reliability stress testing is considered destructive testing, and these parts are not shipped.

Determination of operating conditions and the Absolute Maximum Ratings (AMRs) are the responsibility of suppliers. AMRs may be listed on the data sheet, specifying to customers to never allow stresses to exceed these known limits. A customer may choose to operate the product slightly above the operating conditions for short times, realizing that reliable lifetime is being compromised. But parts stressed beyond AMR limits may become unpredictably unreliable. Additional failure mechanisms may become active. Permanent alteration in the materials occur. It is the customer's responsibility to preserve the product reliability by operating within the specified limits, and especially to never allow stress to exceed AMR limits. Methods for AMR determination are not consistent among suppliers, and interpretation of AMRs by customers vary widely. The ESD Association is currently conducting research, intended to aid both suppliers and customers in determination, specification and interpretation of AMRs for best success in reliable product use.



Stevan Hunter, PhD, is Reliability Engineering Consultant and ESD Control Champion at ON Semiconductor in Phoenix, Arizona, USA, with 40 years of experience in Semiconductor engineering. He also manages university research projects for ON, and teaches as Faculty Associate at ASU, BYU-Idaho and UMD CALCE.

"Technology Trends for Large Area Panel Level Packaging"
Dr. Tanja Braun, Lead of Assembly & Encapsulation Technologies in Fraunhofer IZM.

Panel Level packaging (PLP) is one of the latest packaging trends in microelectronics. Besides technology developments towards heterogeneous integration also larger substrates formats are targeted. Fan-out Wafer Level manufacturing is currently done on wafer level up to 12"/300 mm and 330 mm respectively. For higher productivity and therewith lower costs larger form factors are introduced. Instead of following the wafer level roadmaps to 450 mm, panel level packaging might be the next big step. Easy upscaling of technology when moving from wafer to panel level as well as simple use or adaptation of existing large area tools and materials as e.g. from Printed Circuit Board (PCB) or Liquid Crystal Display (LCD) manufacturing is not possible. Additionally the missing standardization in sizes is another challenges. Considered panel dimensions ranges from 300x300 mm² to 457x610 mm³ or 510x515 mm² up to 600x600 mm² or even larger.
When moving from wafer to panel level materials, equipment and processes have to be further developed or at least adapted. A view along the process chain offers lots of possibilities but also challenges. Starting from carrier material selection for a chip first approach where not only the thermo-mechanical behavior but also properties as e.g. weight or stability should be considered. Pick and place assembly on carrier is independent from wafer or panel formats a bottleneck. Here new equipment or even new approaches for high speed but also high accuracy assembly are required. Compression molding is typically used for chip embedding and to form the reconfigured wafer or panel. Liquid, granular and sheet type molding compounds are available. All allowing chip embedding with pros and cons in cost, process ability but also in cleanroom compatibility. For redistribution layer (RDL) formation a large variety of lithography tools and dielectric material options exist. As dielectrics photosensitive as well as non-photosensitive or liquid versus dry-film materials can be considered. Mask-based lithography as e.g. stepper technology is just as maskless based tools as laser direct imaging (LDI) available for panel sizes. Both offering different capabilities and strategies to overcome challenges from die placement accuracy and die shift after molding. Finally also solutions for grinding, balling and singulation are needed. Handling and especially

automated handling of molded large panels including also storage and transport is still an open topic as until now only custom-made solutions exist.
However, in addition to the technical challenges also the question where is the sweet spot for large area panel level packaging is not fully answered. Here cost modelling can help to better understand overall cost structure and process and equipment assembly related to different application scenarios.

Dr. Tanja Braun studied mechanical engineering at Technical University of Berlin with a focus on polymers and micro systems and joined Fraunhofer IZM in 1999. Since 2000 she is working with the group Assembly & Encapsulation Technologies and since 2016 she is head of this group. Her field of research is process development of assembly and encapsulation processes, the qualification of these processes using both non-destructive and destructive tools and advanced polymer analysis. Recent research is focused on wafer and panel level packaging technologies and Tanja Braun is leading the Fan-out Panel Level Packaging Consortium at Fraunhofer IZM Berlin. In 2013 she received her Dr. degree from the Technical University of Berlin for the work focusing on humidity diffusion through particle-filled epoxy resins. Results of her research concerning packaging for advanced packages have been presented at multiple international conferences. Tanja Braun holds also several patents in the field of advanced packaging. In 2014 she received the Fraunhofer IZM research award

“Low temperature interconnect technology using Sn-Bi alloy system for high performance packages”

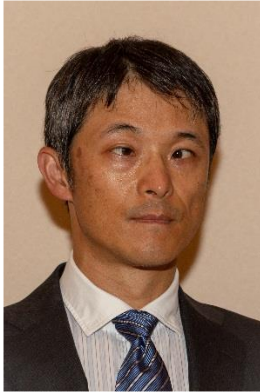
Mr. Kei Murayama, R&D in SHINKO ELECTRIC INDUSTRIES CO., LTD.

Recent years, a low temperature interconnection using Sn-Bi solder has received remarkable attention from semiconductor packaging and SMT industry. Because high temperature warpage induces reducing yield during solder reflow. And in case of large size die application, CTE mismatch between a silicon die and an organic substrate induce large stress at solder interconnection. In addition, electro-migration phenomenon is the most significant problem for high performance packages. The current density at the micro solder joint is expected to be in the order of 10kA/cm2. In case of Sn3.0wt.%Ag0.5wt.%Cu (SAC) solder which is conventional lead-free solder, large cracks are formed at the cathode interface after current stressing. On the other hand, in case of Sn-Bi solder, vacancy or crack is not formed at the cathode interface even after long time current stressing. Sn-Bi solder is strong candidate materials to improve package reliability.

Firstly, we introduce the difference of warpage behavior and stress change between Sn 57 wt.% Bi (Sn57Bi) solder and SAC solder in the flip chip interconnection area using a large die (20 × 20 mm). The reflow peak temperature of Sn57Bi solder and that of SAC solder were 180 degrees C. and 245 degrees C., respectively. The warpage after chip mounting using Sn57Bi solder and that of using SAC solder were 36.0 μm and 96.5 μm, respectively. And microstructure and strain analyses of the flip chip interconnection area were performed on both Sn57Bi and SAC solder by Electron backscattered diffraction (EBSD). Regarding initial state of SAC solder, at the corner bump, the average grain size of β-Sn was 28.8 μm. After thermal cycling (TC) test, the average grain size of β-Sn was refined less than 6 μm. Regarding Sn57Bi solder, at the initial state, the average grain size of β-Sn at all location was less than 4.4 μm. After Thermal cycling (TC) test, the average grain size of β-Sn was less than 4.5 μm. Refining of β-Sn was hardly observed. We employed Grain Reference Orientation Deviation (GROD) analysis for strain analysis. As the plastic strain increases, the GROD value increases. In the case of initial state of SAC solder, high angles were observed at the corner bump and strain concentration were observed at the edge of Cu pillar and at the edge of substrate pad. After TC test, crack propagation was observed at the same point. On the other hand, in the case of Sn57Bi solder, high angles were less than 3 % and strain concentration were not observed. After TC test, crack propagation was not observed. These results suggest that using Sn57Bi solder is less affected by thermal stress than using SAC solder.

Secondly, we introduce the difference of electro-migration mechanism between SAC and Sn-Bi solder. The current density was 40KA/cm2 and test temperature were 150 degrees C.(SAC) and 125 degrees C.(Sn-Bi), respectively. In the case of SAC solder, the resistance change was hardly observed at 100 hours. But the resistance rapidly has increased and the electrically open failure was observed at 140 hours. Sn atoms migrated to the anode side by the electron flow but the metal atoms hardly move by the back flow. Crack were formed at the cathode interface. On the other hand, Sn57Bi solder showed the behavior that was different from SAC solder. The resistance had gradually increased to 25 % at 100 hours. And after, the resistance had gently increased to 80 % at 3300 hours. Bi atoms migrated to the anode side and accumulated on Cu pillar by the electron flow. And Sn atoms migrated to the cathode side by the back flow. However, vacancy or crack was not formed at the cathode interface. Because resistivity of Bi is higher than Sn, resistivity change of Sn-Bi system was affected by Bi content. In the case of Sn30wt.%Bi(Sn30Bi), the resistance change was less than 20% at 2000 hours. Sn30Bi solder showed high electro-migration resistivity. We also introduce 2.5D

application using Sn-Bi solder. Sn-Bi solder has employed for interconnection between an interposer and an organic substrate. We found that using Sn-Bi solder can reduce the warpage and the solder interconnection stress.



Kei Murayama received his B.E. and M.E. degrees in chemical engineering from Shinshu University, Nagano, Japan in 1991 and 1993, respectively.
He joined SHINKO ELECTRIC INDUSTRIES CO., LTD. in 1993.
He has been engaged in the research and development of semiconductor packaging. He has 25 years of experience in semiconductor packaging industry and has worked in various interconnect techniques and packaging techniques such as solder ball formation, flip chip bonding, TLP bonding, silicon package, silicon interposer, wafer bonding and HS attach.
His current research interests include a low temperature and a low stress bonding for high performance package such as organic interposer. He is mainly working on the development of flip chip bonding technique using low temperature solder and elucidation of its electro-migration phenomenon.
And his current interests also include microstructure and crystal orientation analyses of the interconnection bump by Electron probe micro analyzer (EPMA) and Electron backscattered diffraction (EBSD).

"Microfluidic Electroless Interconnection Process for Low-Temperature, Pressureless Chip-stacking"

Prof. C. ROBERT KAO, program manager of Materials Engineering in Ministry of Science and Technology of Taiwan.

Increasing demands for high-performance miniaturized electronic devices have driven the semiconductor industry toward finer pitch and higher interconnect density. Copper pillar has been widely adopted and is rapid becoming the mainstream bumping technology for high-density interconnections, such as 2.5D and 3D IC packaging. Thermo-compression bonding has been widely used for high-density copper pillar bumps because of its highly accuracy alignment and placement. However, the high heat and high force applied to the components during the bonding process often induce high thermal-mechanical stress that causes severe damage to the devices and low-k dielectric layers. Because the mechanical properties of porous, low-k materials decreases with lower dielectric constants, this issue will become more severe in the future when lower dielectric constant materials are employed. Therefore, it is imperative to develop a low-temperature, low-pressure bonding process.

To address this issue, a novel Cu-to-Cu bonding process called microfluidic electroless interconnection has been developed. This novel process forms electroless metal interconnections as a replacement for solders, which eliminates all the reliability concerns involved with soldering. Specifically, the process is able to bond copper pillars at a low temperature without applied any pressure. The operating temperature of the process is around 80 °C, which is considerably lower than most bonding processes. Also, there is no need to apply any bonding pressure throughout the bonding process due to the proposed bonding scheme structure. In this way, the thermo-mechanical stress can be largely reduced to maintain the structural stability of packaging. Furthermore, the most exciting aspect of this new approach is the integration of microfluidic technology with the electroless plating process, which allows to precise control the flow of fluids in and out the stacked chip to achieve better bonding performance. The flow rate can quantitatively determined and the fluid flow can be adjusted for either batch or continuous-flow operations.

The main objective of this work was to investigate the feasibility of the microfluidic electroless interconnection process in joining copper pillars as a promising route for a low-temperature, pressureless bonding process. First, the overall plating uniformity across the entire die surface at different stand-off heights of the stacked chips was investigated. Preliminary results demonstrated that, by selecting a proper flow rate, a high level of plating uniformity across the die was obtained regardless of the standoff heights. In addition to the electrolessly bonded joints, when the bonding interface was examined by scanning electron microscopy (SEM) and focus ion beam (FIB), it was confirmed that no voids or seams appeared on the bonding interface between the pillars, indicating that the two electroless Ni layers that grew on the opposite sides had merged completely into a single structure. The growth and bonding mechanism of the electroless interconnection process was investigated and characterized fully. The bonding interface and phosphorus distribution in the electroless Ni bonds were examined by an electron probe micro-analyzer (EPMA) to ascertain the effect of batch and continuous flow processing. Moreover, the results of direct shear test shows that the bond strength of the electroless Ni between the copper pillars was greater than the adhesion strength of the Cr layer. Further, it was found that the process has the ability to compensate not only for non-uniform copper surfaces, but also for the misalignment and height mismatch of copper pillars, which provides a competitive edge over other bonding methods. This innovative low-temperature, pressureless electroless bonding approach shows considerable promise for applications that require low stress and low thermal budget process.

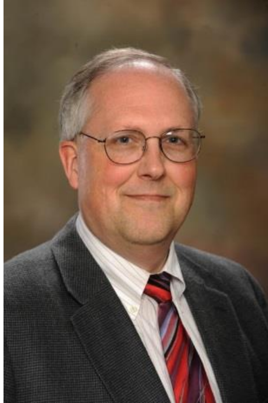
C. ROBERT KAO (SM'11) received his PhD in Materials Science from University of Wisconsin-Madison in 1994. He joined National Central University (Taiwan) in 1995 as an assistant professor. In 2005, he became the first director for the newly established Graduate Institute of Materials Science & Engineering at National Central University. In 2006 he

relocated to National Taiwan University, became a University Distinguished Professor in 2008, and served as the Department Head of Materials Science and Engineering from 2010 to 2013. He currently also serves as the program manager of Materials Engineering in Ministry of Science and Technology of Taiwan. His main research interests include electronic, optical, and MEMS packaging with a main thrust on the thermodynamics and kinetics of materials interactions within packages. He helped organizing 16 international symposia on solders and soldering technology for TMS and ASM. He has served as guest editors for Journal of Electronic Materials and Microelectronic Reliability, and currently is a Principal Editor for Journal of Materials Research and Associate Editor for Journal of Materials Science – Materials in Electronics. Kao is a committee member for CPMT Materials and Processing Technical Committee, and also served as session chair for ECTC meeting.
Kao is a Fellow of the ASM and MRS-Taiwan. In 2014, he received the Brimacombe Medalist Award from TMS. He is a High Impact Research Icon of University of Malaya, Kuala Lumpur. He has authored over 130 referred journal papers, five of which reached the status of Highly Cited Papers according to Web of Science Essential Science Indicators. He has an h-index of 33. He holds 10 US and Taiwan patents. Kao is considered the leading experts on the metallurgical reactions for electronic packaging applications, and has given more than 30 invited or keynote lectures in international conferences. He presented an invited talk at the Gordon Research Conference (Plymouth State College, July 23-28, 2000), and served as a discussion leader for the same conference in 2006. In addition to his teaching and research activities, Professor Kao was an independent board member of LOTES (2006-2010), and served as consultants for many industry leading corporations, including ASUS and VIA Technologies

"Effects of Aging on the Reliability of Electronic Products Incorporating Lead Free Solders"
Prof. Jeffrey C. Suhling, Mechanical Engineering at Auburn University. Board of Governors IEEE Electronics Packaging Society.

Environmental concerns and legislation adopted in Europe and Asia has led to a nearly universal world-wide transition to lead free solders (so-called SAC alloys) in electronic products over the past 15 years. One of the greatest challenges has been that lead free solders are highly susceptible to aging effects, where their mechanical behavior and failure properties degrade with time when exposed to isothermal or variable temperature environments. Such degradations are caused by the unstable microstructures present at very low temperatures, and they can lead to a significant reduction in the reliability of electronic products with time.
In this talk, an overview of our research on the effects of aging on the mechanical behavior of lead free solders is presented. This work as involved a combination of experimental material characterization and measurements of microstructural evolution, as well as constitutive model development and finite element predictions of reliability. Stress-strain and creep tests have been performed using miniature tensile samples, and the degradations in the effective elastic modulus, yield stress, ultimate tensile strength, and creep strain rate have been characterized and modeled as a function of aging temperature, aging time, and alloy composition. Analogous results have also been obtained using nanoindentation testing of small solder joints from non-aged and aged lead free electronic assemblies. Finally, cyclic stress-strain testing has been utilized to understand the aging induced degradations in the hysteresis loop and fatigue life. The results of the experimental mechanical testing have

been correlated with observations of microstructural evolution occurring in lead free solders during aging to develop a fundamental understanding of the causes of the material property degradations. In addition, methods to mitigate aging effects have been developed through the use of microalloy additions. Finally, the measured data have been used to build aging effects into the Anand viscoplastic constitutive model as well as a modified Morrow model for fatigue life, and then implemented in finite element simulations to make reliability predictions for electronic products subjected to aging.



Jeffrey C. Suhling received his Ph.D. degree in Engineering Mechanics in 1985 from the University of Wisconsin. He then joined the Department of Mechanical Engineering at Auburn University, where he currently holds the rank of Quina Distinguished Professor and Department Chair. From 2002-2008, he served as Center Director for the NSF Center for Advance Vehicle Electronics. His research interests include solid mechanics, stress and strain analysis, material characterization, experimental mechanics, advanced and composite materials, finite element analysis and computational mechanics, additive manufacturing, electronic packaging, and silicon sensors. Dr. Suhling has authored or co-authored over 400 technical publications, and he has advised over 80 graduate students at Auburn University. He is a Fellow of ASME, and is a member of IEEE, SMTA, IMAPS, SEM, and TAPPI. He served as Chair of the Electrical and Electronic Packaging Division of ASME during 2002-2003, and was on the EPPD Executive Committee from 1998-2003. Dr. Suhling was the Technical Program Chair of the ASME InterPACK '07 Conference, and General Chair of the ASME InterPACK '09 Conference. He currently serves on the IEEE Electronics Packaging Society Board of Governors, and is the General Chair of the 2019 IEEE ITherm Conference

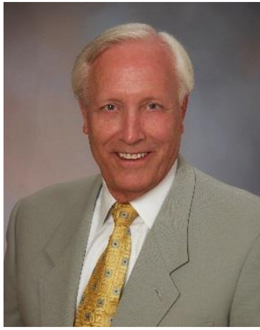
"Interface Pattern Void Analysis in Face to Face Hybrid Wafer Bonding"
Dr. Soon-Wook Kim, Senior Process Integration Engineer at IMEC.

Various technologies have been approached and explored to integrate different system partitioning schemes for the advanced chip-level or wafer-level packaging [1]. In a view point of 3-D SoC applications, hybrid wafer to wafer (W2W) bonding by directly stacking BEOL layers from two damascened wafers would be a preferable option to achieve high interconnect density. Recently the sub-micron pitch feasibility in hybrid W2W bonding technology has been demonstrated by the electrical interconnection results and cross section [2]. However, the comprehension of surface topography prior to wafer bonding is not enough to control the interface void defectivity, which is relevant with designed structure layout not with random defectivity such as surface particles and contaminates. In other words, the pattern voids have not yet been studied as quantitatively to provide the basic pad layout design guideline for hybrid wafer bonding. Hence, this paper presents the correlation of interface pattern voids and nano topography by using scanning acoustic microscope (SAM) and inline atomic force microscope (AFM).
Test material has been prepared and evaluated by 300 mm wafer-level bonding procedure as introduced in the previous our study [3]. Figure 1 illustrates our noble design and integration concept for face-to-face hybrid wafer bonding [4]. The pre-bonding surface topography was characterized by inline AFM metrology which enables the analyzed wafers to be bonded as non-destructive characteristics method. The bonded wafers were inspected by wafer-level c-SAM to investigate the interface bonding voids. Figure 2 shows the typical SAM image and the test structures' void defect category, pass and fail. The obtained SAM data were quantitatively analyzed by image recognition coding through every test structures across the whole wafer dies. Thanks to this internally developed program script, the bonding yield of each test structure was statistically collected. Figure 3 shows the strong dependence of bonding yield on Cu pad density (pitch). To verify the effect of test structure topography on pattern voids, the integrated device wafer was stacked with the identical process wafer except the patterning process. Figure 4 shows this type result of bonding void wafer map of 1.08um Cu pad array of 50% density. The device pattern topography was analyzed by the inline AFM data prior to bonding. Figure 5 shows the scanned AFM data, and the dielectric profile and the derivative values in terms of slope change around the pad array.
To look into the correlation of Cu size and density concerning to interface pattern voids, the bonding yields were represented by variable size and density using a color scale as shown Figure 6. The pattern voids were not detected in case that the Cu pad size was limited below 2μm as keeping the lower Cu array density than 25-35%. In the good bonding structure 720nm Cu of 25% density, the dielectric profile slope was less than 1 nm/μm.
Pattern voids placed at wafer bonding interface have been investigated according to Cu pad design window for hybrid W2W bonding technology. To avoid the interface pattern bonding voids the low Cu density as less than 25% is proposed together smaller pad size than 2 μm as design guideline.

Soon-Wook Kim is senior process integration engineer at IMEC. He presently performs R&D in the field of hybrid wafer bonding focused on 3D System-On-Chip (SOC) integration for 5 years. Before joining IMEC, he took on the role of 2.5D integration project in Institute of Microelectronics (IME, Singapore). He started the semiconductor various activities at Hynix System IC research center in 2003 and his main focus is back-end-of-line (BEOL) interconnection as well as CMOS passive device. He had also experienced the 0.18um analog/mixed-signal product development in MagnaChip Semiconductor, spin-off from Hynix until 2011. Soon-Wook Kim obtained a master degree in 1999 and PhD in 2003, both in Material Science and Engineering from Hanyang University (Seoul, Korea).

"Package Level Systems Integration: A key to maintaining the pace of progress"
Dr. Bottoms, Chairman of Third Millennium Test Solutions.

The most efficient path for progress in electronic systems for more than 50 years has been Moore's Law scaling but the advantages of scaling CMOS are now approaching their economic end. Information technology must identify new approaches if the economic and societal benefits are to maintain their pace of progress in the post Moore's Law era. This need has accelerated innovation in new technologies to maintain the improvements in size, cost, performance and power efficiency that has driven information technology into every corner of human activity over the last 50 years. The coming changes are evident with evolutionary progress in advanced packaging, introduction of new system architectures, new device types, new materials and new processes for both design and production. The evolution includes wafer level packaging, 3D integration and heterogeneous integration of known components into a single package.
The revolution that is just beginning will include a complete remake of the global network, new devices for both logic and memory functions, an array of sensors of all types. The emergence of big data, the internet of things and migration of memory, logic and applications to the cloud are moving the majority of power usage from logic towards memory transport. The path toward maintaining the pace of progress for decades to come will, however, transform this evolution in the industry to an industrial revolution where new device types and other components are integrated into systems at the package level. The ultimate realization of this revolution will be full system integration of complex products in the package. There are difficult challenges that must be overcome to realize this revolution. Many of the elements of this revolution are in development today and will be discussed in this presentation.



Dr. Bottoms received a B.S. degree in Physics from Huntington College in Montgomery, Alabama in 1965, and a Ph.D in Solid State from Tulane University in New Orleans in 1969 and is currently Chairman of Third Millennium Test Solutions. He has worked as a faculty member in the department of electrical engineering at Princeton University, manager of Research and Development at Varian Associates, founding President of the Semiconductor Equipment Group of Varian Associates and general Partner of Patricof & Co. Ventures.

Dr. Bottoms has participated in the start-up and growth of many companies through his venture capital activity and through his own work as an entrepreneur.

He has served as Chairman and CEO of many companies both public and currently serves as: Emeritus Member of the Board of Tulane University, Co-Chair of the Heterogeneous Integration Roadmap, Chairman of the SEMI's Awards Committee, Chairman of the Packaging and Package Substrates Technical Working Group for INEMI, Member of the Board of MIT's Microphotonic Center, Chairman of Fluence Analytics, Chairman of Third Millennium Test Solutions.

“Organic substrate material with low transmission loss and effective in suppressing package warpage for 5G application”

Mr. Shunsuke Tonouchi, Laminate Material R&D Dept., Hitachi Chemical Co.

Mobile communication system has been graded up in every decade. The next generation system, which is called 5G, is coming. The data transmission speed of mobile device will be 10 Gbps or higher. Such a high performance infrastructure can change the world and strongly support autonomous, IoT/IoE and other emerging systems. The frequency band used in 5G is now discussing in the standardizing organizations and each government. Some bands of millimeter wave between 20 to 80 GHz are strong candidates. Signal transmission loss is proportional to transferring frequency, and dielectric dissipation factor (Df) and a root of dielectric constant (Dk) of dielectric constant. Dielectric material with low Dk and Df is preferably required for high frequency signal transferring system. The low loss system can suppress the power consumption and heat generation. Thinner form factor is kept demanded in the package of mobile device like smart phone and tablet. Substrate is also required to be thin with the performance of suppressing the package warpage in such an application. Therefore, the package substrate for 5G mobile device will be required to satisfy the low transmission loss and the small package warpage. Low coefficient of thermal expansion (CTE) is known for reducing package warpage, so the substrate material with low CTE is also required. Additionally, other than the package substrate such performance material is also expected for the mother board of mobile device

In this research the substrate material having low Dk and Df, and CTE has been developed. The material is the composite of the originally designed thermosetting resin and the glass fabric. The base resin system is composed of the hard and the soft segment. The former segment consisted of the polycyclic resin having the planer stack structure of aromatic ring. The strong intermolecular force between the stacks restricts the local movement of the resin system, which can contribute to the small CTE and the low Df. The latter segment can make the resin component follow the thermal behavior of the glass fabric which is a small CTE material. Consequently, the composite material can show the very small CTE which is close to that of the glass fabric. Moreover, the low elastic modulus of the resin system, which is derived from the latter segment, works well to lower the residual stress. It is effective in the package warpage suppression. Using low or non polarity component is a basic idea to design low Dk and Df resin system. The hard segment of polycyclic resin has some polarity. In general different polarity components have less compatibility each other. We have overcome the compatibility issue by introducing chemical co-crosslinking reaction modifying both the polycyclic and the low polarity components. Tg, CTE, Dk and Df of the developed composite material are 220 degree C, 6.0 ppm/degree C, 3.5 to 3.6 (@ 10 to 77 GHz) and 0.0035 to 0.0065 (@ 10 to 77GHz), respectively. Tg and CTE were evaluated by thermos mechanical analysis. Dk and Df were measured by triplate resonator method for 10 GHz and cut-off circular waveguide method for 77 GHz. Warpage behavior of the package was evaluated comparing with the conventional coreless thin substrate. The package and the die size were 14 x 14 and 7.3 x 7.3 mm2, respectively. The substrate was 300 um thick and 5 layer coreless structure. Convex warpage was observed at the cooling step after reflow. The warpage value was 150 um. It was smaller than that of the conventional substrate, which was 167 um. Signal transmission property at 28 to 77 GHz was also evaluated by making Cu micro strip line on the substrate. The loss values at 28 and 77 GHz were 0.47 and 1.38 dB/cm, respectively. Those were smaller than the values of the conventional one, which were 0.87 and 2.30 dB/cm, respectively. Better performance of the developed material regarding signal transfer and warpage suppression was clearly shown. And an insulation reliability evaluation of bias-

HAST. 12 Volt bias was applied to the comb electrode of line and space of 30 and 30 um, which was formed on the material. No electrical insulation degradation was observed at 130 degree C and 85%RH for 200 hours

Mr. Shunsuke Tonouchi is currently in Laminate Material R&D Dept., R&D Headquarters, Hitachi Chemical Co., Ltd. He holds Master degree in environmental studies from Tohoku University, Miyagi, Japan, in 2013 after getting Bachelor degree in engineering from Tohoku University, Miyagi, Japan, in 2011. His main study was nanoscience of inorganic chemistry. He has been working in the field of resin design and polymer synthesis for organic substrate material since then.

"Engineering Green Electronics"

Prof. David Mark Harvey, Electronic Engineering at Liverpool John Moores University. UK

The ubiquitous nature of electronics in daily life coupled with the Moore's Law type enhancements in the integrated circuit field now requires serious thinking about how to "green" electronics technology.
Packaging, circuit interconnections and size will keep getting smaller but how far can we move to green-up the business? Design for manufacture, test, reliability, EMC and low power are important considerations, but have we considered how to use more environmentally friendly components and at the end of life methods to reduce landfill through more efficient recycling.
Key to less wastage are more reliable products, and some recent work completed on through-lifetime monitoring of solder interconnections on area array packages will be considered. Lifetime testing of area array packages through both thermal cycling and vibration has started to identify failure mechanisms by imaging the hidden solder balls. Extensive ultrasound scans and some X-ray imaging have helped measure the failure progression from new product to failure.
Failure mechanisms in manufactured electronics are often caused by mismatches in the individual coefficients of thermal extension, differences in stiffness/rigidity, and poor component placement. Can new materials be invented at an appropriate cost to better match up the individual design components and reduce failure/stresses for increased lifetime and more reliable products? If these new materials can also be environmentally friendly and easily recyclable then we have gone some way towards green electronics.
Work completed has started to find failure profiles for lead-free solder joints and examples will be given on real test samples for area array packages lifetime tests and embedded die delamination failure analysis. In future new types of solder will be important and further work on new materials is required here. Some joint work has recently started on design and lifetime analysis new solder materials between Malaysia and the UK through a two-year Newton project.
An important aspect of measuring hidden solder joints or die is to separate the layers to find the exact position of any fault that may occur during lifetime tests. The team have designed an image processing toolbox that can separate overlapped layers in ultrasound scans such that a type of "Data Fracking" using complex wavelets can isolate the depth of previously undetectable faults. So turning a series of 2D horizontal scans into a 3D layered picture.

Dr David Mark Harvey is Professor of Electronic Engineering at Liverpool John Moores University. UK. He conducts research, teaching and enterprise work in digital electronics design, manufacture and test. He has published over 100 articles and successfully supervised 17 PhD students. He has directed two large technology transfer projects funded to €10M, and through these projects worked with over 250 companies. All research work has an industrial bias and the graduates produced have entered industry in the electronics sector.

Of three recent PhD graduates, one is European validation manager for a large multinational automotive electronics company, one is working in product validation at Intel in Penang, and a third entered Cambridge Silicon Radio (now Qualcomm). In the past he has helped set up two design centres in India, and worked for companies in the UK in the steel industry, high vacuum scientific instruments and secure electronic communication. His present interests are in the design, manufacture and test of automotive and space electronics.

"Novel Thin Wafer De-bonding System for 3D TSV Multi-Chip Packaging of High Bandwidth Memory Devices"

Dr. Min Woo Rhee, Program Manager and Principal Engineer in Manufacturing Technology Research and Development Center, Samsung Electronics, South Korea

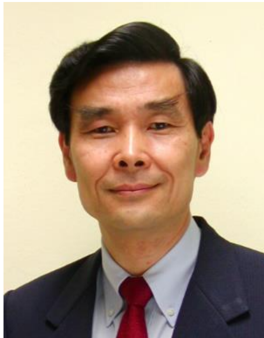
The stable temporary bonding and de-bonding system for 3D IC packaging is one of the most crucial processes to achieve successful 3D HBM memory device stacking by applying TSV (Through Silicon Via) technology. However, there are not much proven de-bonding systems with sufficient stability and reliability to handle less than 50㎛ wafer thickness. To meet those challenges, lots of temporary bonding and de-bonding concepts have been investigated through the 3DIC integration history for both in industry and research. The concept for the first generation was the mechanical de-bonding system using thermoplastic resins which has been widely used above 100㎛ thin wafer handling system such as thermal slide off or lift off type. However, since those de-bonding system inevitably induce huge amount of mechanical stresses on the thin downed wafer it is very difficult to establish stable process condition when the thickness requirement is move down to 50㎛. In addition, since the de-bonding mechanism is often complicit with the material requirement during 3DIC process. It should withstand high temperature and high vacuum process such as dielectric cure and PECVD, even in chemical process. If the adhesion is strong then the reliability of the temporary bonded layer is good enough to withstand various conditions of 3DIC processes, however de-bonding process is too challenging since the adhesion between the bonded pair is already strong. On the contrary, if the adhesion of bonded pair is weak enough to provide easy de-bonding condition, then 3DIC process stability is drastically going down. To overcome those challenges, recently the scientist and researcher are more focused on different process mechanism between temporary bonding and de-bonding, such as temporary bonding by polymer crosslinking and de-bonding process by focused laser between the interfaces of bonded pair, but report has it that this method also have much concerns because it could damage the active layer on the devices. To overcome those technical challenges, the authors suggest novel damage free thin wafer de-bonding system which can apply high power UV irradiation with specific wave length on UV sensitive polymer film on glass carrier wafer. The experimental analysis shows that the developed system is able to de-bond the thin wafer from the carrier with no damage and sufficient productivity for mass production.

Min Woo Rhee was born in Seoul, South Korea, in 1973. He received the B.Eng. (Hons.), M.Sc., and the Ph.D. degrees in chemical engineering from Sogang University, Seoul, and the master's degree in management of technology from National University of Singapore (NUS), Singapore. He has about 20 years' experience in microelectronics packaging research and development for both industry and research institutes. He also has extensive experience in advanced packaging and material development, modeling and characterization. He was also with Amkor Technology Research and Development from 1999 to 2010, where he was the Senior Manager and the Leader of the Material Characterization Modeling and Failure Analysis Group. He also resolved lots of chronic failure and quality issues with the worldwide semiconductor companies. He is currently working as the Program Manager and a Principal Engineer with the Manufacturing Technology Research and Development Center, Samsung Electronics, Hwasung, South Korea. Before his joining Samsung Electronics, he was a Scientist and the Group Leader in interconnection and advanced packaging program (IPP) with the Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR), Singapore. During his working periods in IME A*STAR from 2011 to 2015, he led power module, ruggedized electronics research groups, and industry consortium projects for automotive, oil and gas, deep sea exploration, and aerospace industries. He also has project leading experience on lots of public funded and industry projects related to material and advanced packaging development, such as MEMs, 3-D-IC and fan-out wafer level packaging. In addition, he had developed an automotive three-phase inverter module for power electronics with the Fairchild Semiconductor Research and Development Group as a Principal Engineer, which were successfully implemented for mass production in major automotive industries. He is the author and co-author of 65 journals and conference papers and has more than 20 patents related with microelectronics and advanced packaging area. Also he is the winner of "the Future Creator Award" from Samsung Electronics in 2018 and the "Best Employee of the Year" Award when he was with Amkor in 2009.

"Thermal and Failure Analysis of Advanced Sub-Micron Devices Using Transient Thermoreflectance Thermography"

Prof. Andrew Tay, Adjunct Fellow in the Singapore University of Technology and Design

Thermal characterization of sub-micron devices, detecting sub-micron time-dependent thermal defects and identifying those that represent potential device failures is a challenge in the thermal analysis of today's complex electronic devices. The scaling of device features results in a significant reduction in time response and an increased sensitivity to transient events. With today's complex devices very small localized temperature 'hot spots' can occur due to an unintended functional anomaly in a circuit with a tight design margin or a timing perturbation resulting from a small change in capacitance or another parameter elsewhere in the circuit. As device features continue to shrink so do the challenges of detecting circuit-induced thermal defects. While gaining a full understanding of the device thermal behavior is getting more difficult, extremely high power densities are increasing the importance of having this understanding. Clearly just having average temperature rise information is not sufficient, it is necessary to have a clear understanding of temperature distributions with submicron resolution to detect local hotspots and nanosecond, and even picosecond, temporal resolution to observe time-dependent thermal events with today's high-speed devices.
In this presentation, an overview of the merits and demerits of various techniques for measuring device thermal behavior will be presented. Thermoreflectance thermography (TRT) will then be described in greater detail and it will be shown how it can be used to thermally analyze today's device structures using illumination wavelengths in the visible range. This imaging technique enables spatial resolution of down to 0.25 micron and when combined with temporal resolution in the nanosecond range meets the requirements necessary to fully characterize the thermal behavior of today's advanced complex device structures. Several case studies will be described.



Dr Andrew Tay is an Adjunct Fellow at the Singapore University of Technology and Design and a technical consultant. He is a former Professor of Mechanical Engineering at the National University of Singapore. Dr Tay obtained his B.E. (Hons I and University Medal) and PhD in Mechanical Engineering from the University of New South Wales, Australia. His research interests include electronics packaging (thermo-mechanical failures, delamination, effects of moisture, solder joint reliability, TSVs); thermal management of electronic systems and EV batteries, thermoreflectance thermography, solar photovoltaics and fracture mechanics. He is currently the IEEE EPS Director of Student Programs, a member of the EPS Board of Governors, the Chairman of the IEEE Singapore Reliability/EP/ED Joint Chapter, and Chairman of the EPTC Board. He was the inaugural General Chair of the 1st Electronics Packaging Technology Conference (EPTC) in 1997. He has served or is still serving in the International Advisory Boards and Organising committees of several regular

international electronics packaging conferences such as DTIP, ECTC, EMAP, EPTC, EuroSime, HDP, ICEPT, IEMT, IMPACT, InterPack, ITHERM and THERMINIC.
For his exceptional technical achievements, he was awarded the 2012 IEEE CPMT Exceptional Technical Achievement Award, and for his contributions to IEEE CPMT Society Region 10, the 2012 IEEE CPMT Regional Contributions Award. For his outstanding contributions in the application of engineering mechanics to electronics and/or photonics packaging, he was awarded the ASME EPPD Engineering Mechanics Award in 2004. He was also awarded an IEEE Third Millennium Medal in 2000. He is a Fellow of ASME and a member of IEEE.