2nd Call for Registration

ABOUT EPTC

The 23rd IEEE Electronics Packaging Technology Conference (EPTC2021) is an international event organized by the IEEE RS/EPS/EDS Singapore Chapter and co-sponsored by IEEE Electronics Packaging Society (EPS). It aims to provide a platform for disseminating innovations and new developments in semiconductor packaging and component technology, from design to manufacturing. Since its inauguration in 1997, EPTC has been established as a highly reputed electronics packaging conference and is the EPS flagship conference in the Asia-Pacific Region 10. It covers diverse areas of electronics packaging technology, including modules, components, materials, equipment technology, assembly, reliability, interconnect design, device and systems packaging, heterogeneous integration, wafer-level packaging, flexible electronics, LED, IoT, 5G, autonomous vehicles, photonics, emerging technologies, 2.5D/3D integration, and smart manufacturing. EPTC2021 features keynotes, technology talks, invited presentations, technical presentations, sponsorship & exhibition corners, and virtual networking activities.

The EPTC technical program committee, which consists of more than 100 experts from diverse technology areas in the semiconductor packaging industry, is committed to creating an engaging technical program for the packaging community. Last year, the 22nd EPTC was conducted on a virtual platform due to the pandemic. More than 680 attendees attended from 30 countries worldwide, with 140 video presentations across the 26 technical sessions. Additionally, technology talks from industry and academic experts have been introduced. The technical program and technology talks will be supplemented by an exhibition where companies exhibit their latest technologies and products for the packaging community.

Considering the current prevailing pandemic situation, the EPTC organizing committee has decided to hold the 23rd EPTC conference proceedings in a virtual mode with both live presentations (Dec 1-3, 2021) and on-demand presentations (December 1-31, 2021). EPTC 2021 will feature live presentations of Keynotes, Technology Talks, Panel Discussions and an HIR Workshop, on-demand presentations of recorded live presentations, the conference invited presentations, regular technical presentations, and professional development courses.

Registration details for EPCT2021 can be found here and EPTC 2021 Advance program can be found here.

Upon successful registration, you will receive the instructions to access EPTC2021 presentations.

The program highlights are as follows:

KEYNOTES

Advanced Package FAB Solutions for Next-Generation Devices *by* **Seung Wook Yoon**, PhD, MBA

Dr YOON is currently the Corporate VP and Head of Team of Package Technology Strategy and Planning, Samsung Electronics. Before joining Samsung, he was director of group technology strategy, STATS ChipPAC, JCET Group. He also worked as a deputy lab director at the Institute of Microelectronics, A*STAR, Singapore. ”Yoon” received a PhD degree in Materials Science and Engineering from KAIST, Korea. He also holds an MBA degree from Nanyang Business School, Singapore. He has over 300 journal papers, conference papers, trade journal papers, and over 20 US patents on microelectronic materials and electronics packaging. He has served as a technical committee member of various international packaging technology conferences, EPTC, ESTC, iMAPS, IWLPC and SEMI.

Abstract: SAMSUNG Advanced Package FAB solutions provide complementary and extended solutions with complete supply chain management, including Fanout WLP, Panel level PKG, 2.5D as well as 3D integration. Currently, higher computing power and memory bandwidth are the major requirements of Al and GPU, accelerators and network devices. These demands lead to the adoption of advanced packaging technologies to increase bandwidth density, thermal performance and to improve electrical performance with shorter interconnection length. 3D TSV technologies provide high bandwidth density within a limited footprint. For HPC applications, 2.5D and 3D technologies are employed for cloud and artificial intelligence (AI). High-performance chip size continues to increase up to one reticle size, and the cost of the leading-edge silicon node is recently soaring. So various chiplet packaging solutions, such as 2D, 2.5D and 3D, are necessary to develop fine pitch interconnection evolutions with the Cu hybrid bonding or fine pitch microbump bonding process. In this presentation, the above-mentioned advanced package FAB solutions are to be introduced and discussed in terms of challenges and opportunities for emerging high-end computing and mobile processor platforms. Furthermore, Fanout WLP, RDL interposer, high-performance 3D SIP and Integrated Stacked Capacitor (ISC) are introduced.

Future Directions for 3D Integration Technologies, Enabling Further Electronic System-Level Scaling Benefits *by* **Eric Beyne,** PhD.

Dr Eric Beyne is Senior Fellow, VP R&D and Program Director 3D System Integration Program, IMEC. Eric obtained a degree in electrical engineering in 1983 and a PhD in Applied Sciences in 1990, both from the Katholieke Universiteit Leuven, Belgium. Since 1986 he has been with IMEC in Leuven, Belgium, where he has worked on advanced packaging and interconnect technologies.

TECHNOLOGY TALKS

A Roadmap Based on a Holistic Understanding of Thermo-mechanical Challenges from Package to System to Maximize Silicon Performance *by* **Gamal Refai-Ahmed**,

Dr Gamal Refai-Ahmed, Life Fellow ASME, Fellow IEEE, Fellow Canadian Academy of Engineering, is Xilinx Fellow and Chief Thermo-Mechanical Architect. He obtained the Ph.D. degree in Mechanical Engineering from the University of Waterloo. He has been recognized as one of the global technology leaders of thermal management through his numerous publications (more than 100 publications) and patents & patents pending US (more than 60) and International (more than 120). His contributions are seen in several generations of both GPU and FPGA products.

State University of New York, Binghamton University awarded him the Innovation Partner Award for his industrial role with Binghamton University. Gamal is the recipient of the 2008 excellent thermal management award, 2010 Calvin Lecture and 2013 K16- Clock award in recognition for his scientific contributions and leadership of promoting the best electronics packaging engineering practice. In 2014, Gamal received the IEEE Canada R. H. Tanner Industry Leadership for sustained product development and industrial innovation leadership. In 2016, ASME awarded Gamal the ASME Service Award. In continuation to Dr Refai's contributions to the best engineering practice, the State University of New York at Binghamton awarded him the Presidential University medal in 2019, the university's highest recognition honour. Gamal was elected to IEEE Fellow for 2021.

Abstract: For several decades, microelectronic industries and relevant Academic communities have expended a tremendous effort developing packages in accordance with Moore's law, leading to not only many breakthroughs and revolutions in packaging technologies but also repetitive efforts addressing traditional problems. In recent years, the push into the Nanoelectronic era is resulting in an ever-increasing awareness of R&D efforts and business drivers to speed up the development and application of "more than Moore", all of which are based upon or derived from silicon technologies but do not scale with Moore's law. For the optimized performance of Silicon packages, most of the academic-based publications often do not report the optimal configuration of the package considering the non-mathematical or mechanical and manufacturability constraints. With heterogeneous integration of different functionalities on a single chip that lead to ever-increasing localization of the heat, a major challenge in forward-looking roadmaps includes the thermomechanical reliability of the Silicon package. With traditional and commercially available cooling solutions approaching their useful limit, the focus must be shifted towards improving the interfacial resistance, namely TIM1, TIM2 by establishing better contact. The total system package from the active die to the heatsink includes several subsystems sequentially arranged. Each of the subsystem's performance is highly interactive or dependent on the other. This article emphasizes that the interaction of the Die warpage with the elongation and adhesion of thermal interface materials (TIMs) plays a crucial role in determining the limits of Si packaging technologies. This can be seen clearly in such package size of greater than 50mmx50mm, which has a coplanarity of more than 8 mil. This type of package can have be MCM, Chiplets, CoW0s, EMIB or monolithic. Furthermore, this manuscript also forecasts the different cooling techniques of data centers to enable the future higher performance Silicon.

Packaging Materials as a Key Enabler for Future Megatrends *by* **Klemens Brunner,** PhD.

Dr. Klemens Brunner serves as President of Heraeus Electronics, a leading packaging materials supplier in the electronics industry headquartered in Hanau, Germany. Before 2018, he was head of the Marketing & Sales department of Heraeus Electronics. He began his career at Philips Research in the Netherlands, where he worked on LEDs technology development and Philips business group Automotive Lighting in product marketing. He joined Lumileds (formerly a division of Philips) in San Jose, USA as general manager of the business unit Automotive LED and general manager Automotive Lighting Asia Pacific, where he was based in Hong Kong. Klemens Brunner has a PhD in physical chemistry from the University of Vienna.

Abstract: 5G Communications, Renewable Energy generation and Electric Vehicles are megatrends that not only impact our daily lives, but also bring significant changes to the entire electronics semiconductor packaging industry. Continuous miniaturization of semiconductor devices requires more advanced packaging to deliver better electrical performance, smaller footprint and higher reliability. Heraeus Electronics will discuss how materials innovations enable such requirements through breakthroughs in the packaging of devices and address the various technology challenges, from ever-shrinking interconnects for System-In-Package (SiP), to stringent reliability requirements for Power & Automotive electronics.

Hybrid Bonding – State-of-the-Art and Upcoming Requirements *by* **Paul Lindner**

Paul Lindner heads the R&D, product and project management, quality management, business development and process technology departments. Lindner joined the company in 1988 as a mechanical design engineer and has since pioneered various semiconductor and MEMS processing systems, which have set industry standards. His responsibilities included designing semiconductor processing systems and tooling for custom applications, including innovative system designs pioneered in the first commercially available wafer bonders, silicon-on-insulator (SOI) bonding systems, and precision alignment systems for 3D interconnect applications. Prior to his appointment as executive technology director, Lindner established a product management department at EV Group. During that time, he was involved in marketing, sales, manufacturing and on-site process support.

Even though heterogeneous integration is not new to the industry, the packaging aspect has not been the focus on any of the PPAC metric. In recent years the system performance is getting more important, where heterogeneous integration and system-technology co-optimization (STCO) are the key building blocks for future devices, especially in high performance, AI and mobile applications. The presentation will give a short outlook into the session, including key building blocks of technology. Over the last decade fusion and hybrid bonding on wafer level has developed and is now readily available as unit process in most foundry and device manufacturers worldwide. In the current industry transformation away from optimization on planar devices towards system integration and towards 3D stacked devices, bonding technologies are playing a crucial role. While most devices such as image sensors or stacked memory have been designed specifically for 3D integration and bonding, the next technology transformation as a universal high density interconnect technology will also trigger a new integration process. Therefore, wafer-level as well as die-level hybrid bonding technologies are being developed and depending on interconnect density, chip size, system yield and cost, the best fit in terms of integration flow will be selected. In this presentation we will provide an overview on the current industry trends and technological developments both for wafer-to-wafer as well as die-to-wafer hybrid bonding. Key technology differentiators, integration scenarios are discussed with respect to the hybrid bonding schemes.

Innovative Copper Electrodeposition Solutions for High-Density Fanout Package Technology *by*
Bryan Buckalew,

Mr Buckalew is a Technical Director within Lam Research's WETS Product Group. He has been responsible for managing advanced packaging activities for SABRE 3D over the past ten (10) years. His most recent focus has been in the area of Wafer-Level-Packaging (WLP) and Through Silicon Via (TSV). Mr Buckalew has worked at Lam Research for over twenty (20) year's and has held several technology leadership positions related to damascene and advanced packaging plating. He has authored several technical papers and presentations and currently has over sixty (60) US patents related to innovations in advanced packaging and electrodeposition technology. Prior to joining Lam Research, Mr Buckalew attended UC Berkeley, where he received his graduate degree in Materials Science.

Abstract: IC packaging technology has evolved in a quite diverse manner over the past decade, addressing both high-end and low-end applications, resulting in approaches such as package-on-package (PoP), high-density fan-out wafer-level package (HDFO), 3D IC integration with through-silicon via (TSV), and 2.5D with TSV-Si interposer. HDFO technology comprises conventional under-bump metallization (UBM) and pillar/micro-pillar, as well as new routing/connection applications such as fine-line redistribution layer (RDL) (sub 5x5µm), integrated via-RDL structures, and mega pillars (>100µm). These new applications drive fundamental challenges in electrodeposition. Fine-line RDL applications present challenges for both lithography and electrochemical deposition (ECD) processes. New electroplating technology is required to prevent physical degradation of the fine-line RDL. Cu undercut resulting from the Cu seed etch process can be minimized by using innovative electroplating technology to reduce the thickness of the Cu PVD seed layer. Thermal cracking of the Cu line has also been posed as a key integration challenge and can be overcome with grain engineering of the Cu ECD film. Many of the current HDFO approaches include the adoption of multi-layer RDL which are fabricated from low dielectric polymer passivation layers and Cu ECD lines. Multi-layer RDL patterns can result in significant topography variation, which can impact other process integration challenges such as control of critical dimensions (CDs). To minimize topography variation, a new ECD reactor design is used to provide ultra-uniform Cu ECD. Mega pillars consist of 180-220 mm (200µm average) Cu thickness while standard Cu pillar applications typically vary between 20 and 40µm (30µm average) thickness. The process of plating large features employed as interconnects often encounters mass transport limitations that can curtail the deposition rate. Convection of the electrolyte above the surface of the photoresist, which is largely influenced by the ECD reactor design, is shown to have a pronounced impact on fill times over the range of feature dimensions. Furthermore, some integration requirements for mega pillars warrant extremely high within-die uniformities and flat bump shape. Attaining such high-quality plating performance can greatly minimize the downstream planarization requirements. This presentation will focus on new innovations in Cu ECD processes for fine line RDL, multi-layer RDL, and mega pillar to enable HDFO technology.

Burn-in testing (bit): Predictive Modeling Enables Improving It by **Suhir Ephriam**

Speaker Bio: Ephraim Suhir is on the ***faculty*** of the Portland State University, Portland, OR, USA, Technical University, Vienna, Austria and James Cook University, Queensland, Australia. He is also CEO of a Small Business Innovative Research (SBIR) ERS Co. in Los Altos, CA, USA, is ***Foreign Full Member*** (Academician) of the National Academy of Engineering, Ukraine (he was born in that country); ***Life Fellow*** of the Institute of Electrical and Electronics Engineers (IEEE), the American Society of Mechanical Engineers (ASME), the Society of Optical Engineers (SPIE), and the International Microelectronics and Packaging Society (IMAPS); ***Fellow*** of the American Physical Society (APS), the Institute of Physics (IoP), UK, and the Society of Plastics Engineers (SPE); and ***Associate Fellow*** of the American Institute of Aeronautics and Astronautics (AIAA). Ephraim has authored ***450+ publications*** (patents, technical papers, book chapters, books), presented numerous keynote and invited talks worldwide, and received ***many professional awards***, including the 1996 Bell Laboratories Distinguished Member of Technical Staff (DMTS) Award (for developing effective methods for predicting the reliability of complex structures used in AT&T and Lucent Technologies products), and 2004 ASME Worcester Read Warner Medal (for outstanding contributions to the permanent literature of engineering and laying the foundation of a new discipline "Structural Analysis of Electronic Systems"). Ephraim is the third "Russian American", after S. Timoshenko and I. Sikorsky, who received this prestigious award. His most recent awards are the 2019 IEEE Electronic Packaging Society (EPS) ***Field award*** for seminal contributions to mechanical reliability engineering and modelling of electronic and photonic packages and systems and the 2019 Int. Microelectronic Packaging Society's (IMAPS) ***Lifetime Achievement award*** for making an exceptional, visible, and sustained impact on the microelectronics packaging industry and technology.

Abstract: The objective of this analysis is to explore what could be done to better understand the physics of and eventually to improve the burn-in testing (BIT) technology in electronic manufacturing. Three predictive analytical ("mathematical") models are developed and applied. The model based on the analysis of the infant mortality portion (IMP) of the (non-random) bathtub curve (BTC) suggests that the time derivative of the failure rate at the beginning of this portion could be viewed as a suitable criterion ("figure of merit") to answer the basic question, "to BIT or not to BIT?", of the BIT undertaking. Clearly, if this derivative is zero, the IMP of the BTC is parallel to the time axis, so that the IMP simply does not exist, and no BIT is necessary. In another extreme case, when this derivative is significant (with a "minus" sign, of course), the IMP of the BTC clings to the vertical, failure-rate axis. Although the undesirable "freaks" do exist in such a situation, they could be easily eliminated by a short and low-level BIT. It is assumed that the "unfavorable" material degradation, physics-of-failure, related failure rate (PFR), which increases with time, do not play a role during this initial stage of the IMP of the BTC and is not considered. Only the "favorable", statistic-of-failure related failure rate (SFR) that decreases with time is taken into account in this analysis. The model based on the analysis of the random failure rate (RFR) of the numerous mass-produced components that the manufactured product of interest is comprised of suggests that the above time derivative is, in effect, the variance of the RFR of these components. Their actual failure rates are typically unknown, and could very well vary in a very wide range, from zero to infinity. It is shown that the non-random SFR can be determined from the probability distributions of the random RFR. Finally, it is demonstrated that the model based on the multi-parametric Boltzmann-Arrhenius-Zhurkov (BAZ) equation can be effectively employed to establish the BIT's adequate duration and level, if this failure-oriented-accelerated-testing (FOAT) is found to be necessary. The general concepts are illustrated by calculated data. It is concluded that predictive modeling should always precede the actual BIT and that analytical ("mathematical") modeling should always complement computer simulations. The future work should be focused on the experimental validation and possible extension of the results and recommendations of this analysis and, hopefully and ultimately, on developing practical and effective BIT procedures

ON-DEMAND TECHNOLOGY TALKS

Thermal Management challenges for Advance Packaging in HPC/AI/ML by Dr. Andy C. Mackie

Dr Mackie is the Technology Head for Indium Corporation's Thermal Interface Materials Applications. In his current role, he is focused on identifying thermal material needs and trends for various high-performance applications and the development and testing of innovative solutions to meet the emerging thermal interface material requirements. He also has responsibility for the development of Indium Corporation's Applied Technology Roadmap. Dr Mackie holds a PhD in physical chemistry from the University of Nottingham, UK, and a Master of Science (MSc) in colloid and interfaces science from the University of Bristol, UK. Dr Mackie was involved in several packaging community activities such as the Past President of the IMAPS Empire Chapter (2014 – 2018) and the past member of the Technical Advisory Committee for the annual International Wafer-Level Packaging Conference (IWLPC) run by the SMTA (2008 - 2015); He was also Chair of IPC solder paste task group (responsibly for J-STD-005) (1996 - 2001) and Vice-Chair of IPC Assembly and Joining Materials Subcommittee (1998 - 2002). Dr Mackie is an active member of IEEE, PSMA) Packaging Committee and Society of Automotive Engineers. Dr Mackie is currently the Chair of the Editorial Advisory Board for Chip Scale Review magazine (since 2012), Technical Board member of the Automotive Electronics Council (AEC) (since 2012), and ITRW (International Technology Roadmap for Wide Bandgap Semiconductors) (since 2018).

Abstract: The high-performance computing (HPC) module and AI market is seeing some enormous simultaneous changes. The compute needs of XPU, and tensor processors are causing die area to grow, with higher areal power density, and HBM DRAM stacks are now located immediately adjacent to the processor. The paper discusses how metallic thermal interface materials provide low thermal resistance, high reliability and flexibility for advanced compute modules and systems in both TIM1 (die-lid), TIM 2 (lid-heatsink) and TIM 0 (1.5) (die to heatsink) applications. Reflowed indium as a TIM1 has a nearly two-decade performance record in high volume production, where a combination of CTE matching and very high relative bulk thermal conductivity is highly advantageous. This presentation will discuss the latest developments on indium and other metal alloys as known good solderable solutions that have demonstrated very high bulk thermal conductivity relative to more common polymer TIMs for TIM1 applications, as well as illustrating engineered variations of indium alloys that do not require a solder reflow process, eliminating manufacturing process steps. The discussion also includes metallic TIMs designed for use in TIM0 (TIM1.5) applications with the compression inherent in heat sink attachment with mechanical retention. Novel liquid-metal-based solutions are also under development, and the paper will describe some ways in which gallium alloys are providing ways to resolve some of the conflicting requirements (such as pressure and thinned die and reliability) of emerging applications.

Memory Packaging Trends by Emilie Jolivet

Emilie Jolivet is Director of the Semiconductor & Software Division at Yole Développement (Yole), part of Yole Group of Companies. Emilie manages the expansion of the technical and market expertise of her team. In addition, Emilie's mission focuses on managing business relationships with semiconductor leaders and developing market research and strategy consulting activities. With its previous collaborations at Freescale and EV Group, Emilie developed core expertise dedicated to package & assembly, semiconductor manufacturing, memory and software & computing. Emilie Jolivet holds a master's degree in Applied Physics specializing in Microelectronics from INSA (Toulouse, France) and graduated with an MBA from IAE (Lyon, France).

Abstract: Memory is a critical market in modern data-centric societies and is driven by important megatrends, including mobility, cloud computing, artificial intelligence (AI), and the internet of things (IoT). All these are fuelling the "data-generation explosion" and are responsible for robust growth in memory-bit demand. The memory packaging market follows the same trends that rule the stand-alone memory market and will benefit from the robust growth of memory-bit demand and from the ongoing memory-wafer capacity expansion. Different from the stand-alone memory market that is characterized by strong price volatility, the memory packaging market is less volatile since most of the business is carried out internally by memory IDMs. In 2020, we estimated that less than 30% of the memory packaging revenue is generated by OSATs.

Memory Packaging in China is a key business opportunity for OSATs: the two rising memory players in China – YMTC (NAND) and CXMT (DRAM) – do not have experience in assembly/packaging and must outsource all their packaging to OSATs. We estimate that the OSATs' business opportunity related to these Chinese memory players can grow from <$100M in 2020 to ~$1.1B in 2026 (CAGR20-26 ~55%). Wirebond is the most common memory packaging technology. It accounts for >99% of NAND packaging revenues and nearly 100% of mobile DRAM (LPDDR). Packaging for PC and server DRAM has been progressively migrating from wire bond to flip-chip. The adoption of flip-chip packaging with short interconnects – suitable for low-latency data transfer – will be essential to fully exploit the potential of DDR5 and subsequent DRAM generations. With the ongoing slowdown of Moore's Law and the rise of new advanced packaging techniques, back-end processing has gained more and more importance, and several semiconductor companies are now leveraging on it – rather than on the front-end – to improve the performance, the compactness and the number of functionalities of their IC products. Heterogeneous integration techniques (e.g., TSMC's SoIC) and chipset architectures enabled by novel stacking/bonding approaches have become the must-follow approaches to increase the performance of computing systems through tight integration of logic and memory building blocks.

PANEL

Supply Chain Ecosystem Challenges Impacting Global Electronic Packaging

This panel will cover supply chain trends (e.g. convergence, mergers, and acquisitions), material shortages, equipment limitations, manufacturing capacity, and disruptions (e.g., geopolitical, natural & human resources, regulatory & Environmental Health and Safety). Each of these factors must be taken into consideration when making technical and business decisions. Exacerbating these challenges is the COVID pandemic.

The panel will be chaired by Dr Kitty Pearsall, and panellists include C. P. Hung (ASE), Chun Ho (Nelson) Fan (ASM PT), Jan Vardenman (TechSearch International) and TBD (GlobalFoundries). Details of the Panel at EPTC 2021 will be finalized soon.

Is Artificial Intelligence only a topic for discussion or can manufacturing organization monetize benefits for implementing Artificial Intelligence in their manufacturing environment?

Manufacturing companies currently view AI as a new tool that is either early in the implementation phase or still an R&D tool for advanced analytics. Different companies have adopted different approaches to AI while Smart manufacturing is fully underway in terms of getting information from their equipment and sending it to the cloud. AI has many benefits of being implemented across both in front end and back-end semi. The panel will be discussing topics on how each company is approaching AI differently at different stages of implementation and exploiting AI potential. The macro question will be with a large amount of investments to equipped with AI-ready and continuous effort of R&D into AI / ML, do companies see monetary benefits in this early stages or will this pan out to a longer-term strategy. The objective of this panel session is to share strategies and best practices with Smart manufacturing professionals on how AI methods can harvest solutions in the early stages and how different companies are dealing with the challenges.

The panel will be chaired by Chong Chan Pin (K&S), and panellists will be sourced by the panel chair.

WORKSHOP

Heterogeneous Integration Roadmap (HIR)

The Heterogeneous Integration Roadmap (HIR), released in October 2019, is a roadmap to the future of electronics packaging, identifying technology requirements and potential solutions. The primary objective is to stimulate pre-competitive collaboration between industry, academia, and government to accelerate progress. The roadmap offers professionals, industry, academia, and research institutes a comprehensive, strategic technology forecast over the next 15 years. The HIR also delivers a 25-year projection for heterogeneous integration of Emerging Research Devices and Emerging Research Materials with more comprehensive research and development timelines.

Details of the HIR Workshop at EPTC 2021 will be finalized soon

List of Invited Presentation

[Details of Speaker Biography and Abstract can be found here]

1 

Memory Integration Solution in Advanced Package
Yu Po Wang
SPIL

2 

Hybrid Bonding Technology for high-density 2.5D and 3D IC Integration
Masaya Kawano
Institute of Microelectronics, ASTAR

3 

STT-MRAM Product Reliability and Magnetic Package Shielding Designs to Improve Immunity to External Magnetic Field and RF Sources
Vinayak Bharat Naik, GlobalFoundries

4 

Assessing the Impact of Novel Polymers and Thermal Management in a Power Electronics Module Using Machine Learning Approaches
Vaibhav Bahadur,
The University of Texas, Austin

5 

The Evolution of High-Temperature Pb-free Solder for Die-Attachment in Power Discrete Applications
Sze Pei Lim
Indium Corporation

6 

Challenges and requirements for Seed Layer Deposition on Organic Substrates
Suresh Kumar Singaram,
Evatec SEA

7 

Technology and Market Briefing on Semiconductor Packaging
Favier Shoo
Yole Development

8 

Hybrid Two-Phase Cooling Technology for Next-Generation Datacenters
Raffaele Luca Amalfi
Nokia Bell Labs New Jersey

9 

Material development enabling High-Speed and High-Frequency in Advanced Packaging Applications
Michael Gallagher
DuPont Electronics and Industrial

10 

Fan Out Packaging and its Diversity
John Hunt
ASE

11 

Augmented Finite Element Method (AFEM) for the Linear Steady-state Thermal and Thermomechanical Analysis of Heterogeneous Integration Architectures
Venkatesh Avula
Georgia Institute of Technology

12 

Plasma Dicing - a Key Enabler for Heterogeneous Integration and Hybrid Bonding
Richard Barnett
SPTS

13 

Addressing the Large Field Size Challenges for Small Liner/Space RDL Interposers,
Jinho An,
Applied Material

14-20 Rest of the invited papers updating soon

PROFESSIONAL DEVELOPMENT COURSES (PDC)

Antenna-in-Package (AiP) Technology for Millimeter-Wave Applications; INSTRUCTOR: Y. P. ZHANG, FIEEE , NANYANG TECHNOLOGICAL UNIVERSITY, SINGAPORE

Prof.Yueping ZHANG is a full Professor with the School of Electrical and Electronic Engineering at Nanyang Technological University, Singapore, a Distinguished Lecturer of the IEEE Antennas and Propagation Society (IEEE AP-S), a Member of the IEEE AP-S Paper Award Committee, and a Fellow of IEEE. Prof Zhang has published numerous papers, including two invited and one regular paper in the Proceedings of the IEEE and one invited paper in the IEEE Transactions on Antennas and Propagation. He is the Chinese radio scientist who has published a historical article in an English learned journal such as the IEEE Antennas and Propagation Magazine. He received the 2012 IEEE AP-S Sergei A. Schelkunoff Prize Paper Award.

Prof Zhang delivered the plenary, keynote, and invited speeches at the flagship conferences organized by IEEE, CIE, EurAAP, and IEICE. He received the Best Paper Award from the 2nd IEEE/IET International Symposium on Communication Systems, Networks and Digital Signal Processing, July 18–20, 2000, Bournemouth, UK, the Best Paper Prize from the 3rd IEEE International Workshop on Antenna Technology, March 21–23, 2007, Cambridge, U.K., and the Best Paper Award from the 10th IEEE Global Symposium on Millimetre-Waves, May 24–26, 2017, Hong Kong, China.

Packaging and Heterogeneous Integration for Automotive Electronics, and Advanced Characterization of EMCs; INSTRUCTOR: PRZEMYSLAW GROMALA, ROBERT BOSCH GMBH, GERMANY

Dr.Przemyslaw Gromala is a simulation senior expert at Robert Bosch GmbH, Automotive Electronics in Reutlingen. He is currently leading an international simulation team and FEM verification lab focusing on implementing simulation-driven design for electronic control modules and multi-chip power packaging for hybrid drives. His research activities focus on virtual pre-qualification techniques for the development of electronic control modules and multi-chip power packaging. His technical expertise includes material characterization and modelling, multi-domain and multi-scale simulation incl. Fracture mechanics, verification techniques, prognostics and health management for safety-related electronic smart systems.

Prior to joining Bosch Mr. Gromala worked at the Delphi development center in Krakow, as well as at Infineon research and development center in Dresden. He is an active committee member of the IEEE conferences: ECTC, EuroSimE, ICEPT; ASME: InterPACK. Active committee member of EPoSS – defining R&D and innovation needs as well as policy requirements related to Smart Systems Integration and integrated Micro- and Nanosystems. He holds a PhD in mechanical engineering from the Cracow University of Technology in Poland

Fan-out, Chiplets and Hybrid Bonding; INSTRUCTOR: JOHN H LAU, UNIMICRON TECHNOLOGY CORPORATION

Dr.John H Lau , with more than 40 years of R&D and manufacturing experience in semiconductor packaging, John has published more than 500 peer-reviewed papers, 30 issued and pending US patents, and 22 textbooks on, e.g., Advanced MEMS Packaging (McGraw-Hill, 2010), Reliability of 2D and 3D IC Interconnects (McGraw-Hill, 2011), TSV for 3D Integration, (McGraw-Hill, 2013), 3D IC Integration and Packaging (McGraw-Hill, 2016), Fan-out Wafer-Level Packaging (Springer, 2018), Heterogeneous Integrations (Springer, 2019), Assembly and Reliability of Lead-Free Solder Joints (Springer, 2020), and Semiconductor Advanced Packaging (Springer, 2021). John is an elected ASME Fellow, IEEE Fellow, and IMAPS Fellow.

Flip Chip Interconnect Technologies; INSTRUCTOR: ERIC PERFECTO, IBM CORPORATION AND SHENGMIN WEN, SYNAPTICS INC.

Dr Shengmin Wen is the Principal Package Architect at Synaptics Inc., has more than 20 years of semiconductor industry experience in the areas of Si fabrication technology, advanced packaging and assembly process development, Si and packaging co-design, semiconductor device failure analysis, reliability and qualification, product engineering, testing, and volume production business management. In recent years, he focused on the chip-scale package (CSP), including wire bond, flip chip, wafer-level Fan-In and Fan-out, and panel-level packaging development. In particular, he has extensive and unique experiences in flip-chip assembly technologies that uses fine pitch Cu Pillar bump with both mass reflow and thermal compression processes. He is an expert in package warpage control, substrate technologies, advanced fine pitch flip-chip assembly process, and reliability.

He previously worked at Amkor Technology, where he was a director of the 3D CSP Product Group. Dr Wen received his PhD from Northwestern University, Evanston, IL, USA, researching on fatigue and reliability of electronic materials, where he created and published a science-based fatigue theory. Dr Wen has been actively participating and contributing to industry technical conferences to learn, share, and contribute.

Eric Perfecto has over 39 years of experience working in developing and implementing C4 and advanced Si packages at IBM and GLOBALFOUNDRIES. Responsibilities included UBM and Pb-free solder definition for C4 and u-Pillar interconnect and yield improvements in C4 and 3D wafer finishing. He is currently working at the IBM Nanotech Center. He holds an MS in Chemical Engineering from the University of Illinois and an MS in Operations Research from Union College. Eric has published over 75 external papers, including two best Conference Paper Awards (2006 ESTC and 2008 ICEPT-HDP) and the 1994 Prize Paper Award from CMPT Trans. on Adv. Packaging. He holds 55 US patents and has been honoured with two IBM Outstanding Technical Achievement Awards and an IBM Outstanding Contribution Award for the development of the 3D wafer finishing Process (2014). Eric was the 57th ECTC General Chair in Reno, NV, and the Program Chair at the 55th ECTC. Eric is an IEEE Fellow and has achieved senior member status from IMAPS and the Society of Plastic Engineers. He is an EPS Distinguish Lecturer, the Awards Program Director and elected board member of the Electronics Packaging Society of IEEE.

ESD Impact and Risk on IC Package Technology Development and MEMs Devices; INSTRUCTOR: CHARVAKA DUVVURY, ESD CONSULTANT, IEEE DISTINGUISHED LECTURER

Dr Duvvury received his PhD in Engineering Science from the University of Toledo and has worked for Texas Instruments for 35 years in semiconductor device physics with development work in ESD design. He was elected as TI Fellow in 1997 and as IEEE Fellow in 2008. He has contributed to the industry by offering tutorials at various IEEE sponsored conferences and participating in the EDS DL Program. He served as an editor for TDMR (2001-2011) and is currently serving as the editor for TED. After retiring from TI, he has been working as a technical consultant on ESD design. He is a recipient of the IEEE Electron Devices Society's Education Award (2013), Outstanding Contributions Award from the EOS/ESD Symposium (1990), and Outstanding Industry Mentor Award from the Semiconductor Research Council (1994 and 2012). From 2004-2006 he served on the IEDM CMOS Reliability Sub-committee. He has published over 150 papers in technical journals and conferences and holds US 75 patents. He co-authored and contributed to 5 books. Charvaka has been serving on the Board of Directors of the ESD Association (ESDA) since 1997, promoting ESD education and research at academic institutes. He served twice as General Chairman of the ESD Symposium. He has

been co-founder and co-chair of the Industry Council on ESD since 2006. In 2015, he co-founded iT2 Technologies that utilizes an intelligent software engine for rapid ESD data analysis.

CONFERENCE TOPICS

There are altogether **150 technical presentations** covering important aspects of electronics packaging listed below.

- Advanced Packaging
- TSV/Wafer Level Packaging
- Interconnection Technologies
- Emerging Technologies
- Materials and Processing
- Assembly and Manufacturing Technology
- Electrical Simulation & Characterization
- Mechanical Simulation & Characterization
- Thermal Characterization & Cooling Solutions
- Quality, Reliability & Failure Analysis
- Advanced Optoelectronics and Displays.
- Smart Manufacturing and Equipment Technology

We are particularly grateful for the continued and strong support from our sponsors. Your support have enabled us to carry on with the cause to provide a platform for timely dissemination of the latest technical knowledge to the electronics packaging community.

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MESSAGE

On behalf of the EPTC 2021 organizing committee, I would like to extend our sincere gratitude to all sponsors, exhibitors, media partners, technical committee members for providing their continued generous support despite the current uncertainties and challenging circumstances. I trust everyone is coping well despite the disruptions caused by the pandemic. We are all affected in one way or another, and it is more important than ever to support one another. We also quickly learn that digital transformation has a key role to play, becoming more significant than before. I hope that you will find this EPTC 2021 online experience an enriching one. I am sure we will emerge stronger from this pandemic, and I hope to meet everyone in person in 2022.

Most sincerely,

Gongyue Tang, PhD
Institute of Microelectronics, Singapore

General Chair
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