

Memory Integration Solution in Advanced Package, Yu Po Wang, SPIL

Speaker Bio: Dr Wang is currently Senior Director, CRD Center of SPIL, Taiwan. Dr. Wang received Ph.D. in Mechanical Engineering, State University of New York at Binghamton, New York, U.S.A. Dr. Wang started career at Gintic Institute of Manufacturing Technology in Singapore from 1997. He has jointed SPIL since 1998 and led the R&D advanced packaging design team for leadframe, substrate and wafer form packages development. 1997-1998 Gintic Institute of Manufacturing Technology, Singapore. 1998-Present SPIL, Taiwan. Dr. Wang has strong knowledge and experience in packaging characterization including thermal/ electrical simulation, advanced material(co-development), design and advanced packaging development. He has 83 patents in US

Abstract: The application of artificial intelligence products requires data to be collected/transmitted/stored/calculated, to produce actions that resemble human behaviors. With tremendous data to be process quickly, high performance computing semiconductor is important. The trend of IC packaging is moving to heterogeneous integration to reduce the cost, improve the performance. In response to these problems, packaging technology has been focusing on the development of integrated memory solutions to meet chiplets requirements. Today's report will focus on this trend to present.

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Hybrid Bonding Technology for high density 2.5D and 3D IC Integration, Masaya Kawano, Institute of Microelectronics, ASTAR

Speaker Bio: Dr Kawano received the B.S. and M.S. degrees in nuclear engineering from Osaka University, Japan, and the Ph.D. degree in electronics and applied physics from Tokyo Institute of Technology, Japan, in 1987, 1989, and 2008, respectively. In 1989, he joined NEC Corporation, Tokyo, Japan, where he was involved in cutting-edge research in the areas of infrared image sensors, Cu/low-k BEOL integration, and advanced packaging technologies for 22 years. He was with EV Group Japan from 2011 to 2015 where he worked on wafer bonding, nanoimprint lithography for 3D ICs, image sensors, LED, MEMS applications. He joined Institute of Microelectronics (IME), A*STAR, Singapore, in 2015. He is currently a Senior Scientist with Heterogeneous Integration department where he is working on wafer-to-wafer/chip-to-wafer hybrid bonding, TSV and FOWLP technologies. Dr. Kawano has authored and co-authored more than 20 peer-review journals and has more than 60 US patents granted. He has been invited to give talks and lectures at international conferences and workshops. He is also the recipient of IEEE EPTC Best Interactive Paper Award in 2017, IEEE ESTC Best Paper Award in 2010, 13th SEMI Technology Symposium Award in 2006 for the works on TSV-free interposer, FOWLP, and Stacked-Chip Memory, respectively.

Abstract: Although Moore's Law has been a strong driving force of semiconductor technology evolution, the scaling is almost ending especially for on-chip interconnect density. On the other hand, there is still huge room for package interconnect scaling. Recently hybrid bonding attracts more attention as an enabler of finest inter-chip connection as low as 1um pitch, which has high potential to replace conventional TCB for high-end applications. Hybrid bonding was firstly introduced for BSI CMOS image sensors in 2016 with wafer bonding approach. Industries are now looking for other applications such as high-density memory and high-performance computing with chip-to-wafer hybrid bonding approach. There will be new challenges to overcome especially for bonding yield. Potential root causes of low yield hybrid bonding induced by surface topography can be categorized by defect scale as follows: 1) Lithography shot map may create >10mm scale unbonded area; 2) Metal density non-uniformity within a chip creates pattern related voids; 3) Cu dishing/protrusion and dielectric erosion induced by CMP may create sub 10um scale defects; 4) Nano-scale roughness of dielectric surface lowers the bonding energy at dielectric interface. In this talk, detail of the defect potential root causes and solutions to overcome challenges are discussed

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STT-MRAM Product Reliability and Magnetic Package Shielding Designs to Improve Immunity to External Magnetic Field and RF Sources, Vinayak Bharat Naik, GlobalFoundries

• **Speaker Bio**: Vinayak has received Ph.D. degree in Physics from National University of Singapore in 2011. He is currently a MRAM Device lead at GLOBALFOUNDRIES (2014 to present), Singapore. Prior joining to GLOBALFOUNDRIES, he was working as a Scientist at Agency for Science, Technology and Research (A*STAR), Singapore (2011-2014) on conventional and voltage-controlled STT-MRAM development. He has published 50+ technical papers in international journals/conferences and holds 20+ U.S. patents in the field of non-volatile memory and sensor technologies.

• **Abstract:** In the on-going era of artificial intelligence (AI), Internet of Things (IoT) and autonomous vehicles (AV), the semiconductor industry has actively been developing Spin-Transfer-Torque (STT-MRAM) technology based on perpendicular magnetic tunnel junction (MTJ), aiming for next-generation non-volatile memory applications to replace embedded flash and SRAM technologies. Though embedded MRAM (eMRAM) shows superior performance and radiation-tolerance, magnetic immunity of eMRAM is still the concern because of tampering or unintended exposure to magnetic field. Thus, for realizing the next-generation differentiated products using eMRAM such as connected MCU, emerging AI edge and AR applications, it is crucial to verify the immunity of eMRAM to external magnetic field and RF interference (RFI). In this talk, the superior reliability performance of 22nm FD-SOI embedded MRAM technology collected from package level data, and the magnetic package shielding designs to improve immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of eMRAM to external magnetic field and RF interference immunity of

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Assessing the Impact of Novel Polymers and Thermal Management in a Power Electronics Module Using Machine Learning Approaches, Vaibhav Bahadur, The University of Texas, Austin

• **Speaker Bio:** Vaibhav Bahadur (VB) is an Associate Professor and Carl J. Eckhardt Fellow in Mechanical Engineering at UT Austin. His research interests are in the areas of thermal-fluid sciences, thermal management, materials, and energy-water systems. His research targets a fundamental understanding of thermal-fluid-particle transport phenomena with applications in thermal management, energy, water and environmental protection. Prof. Bahadur has a PhD in Mechanical Engineering from Purdue University and a Postdoc from Harvard University. Additionally, he has 4 years industry R&D experience in GE Global Research and Baker Hughes. Prof. Bahadur is the recipient of the NSF CAREER Award (2017), the SPE Petroleum Engineering Young Faculty Award (2015), the ASME ICNMM Outstanding Early Career Award (2018), the Google Faculty Research Award (2018), and the ACS Doctoral New Investigator Award (2014). He is the winner of the Society of Petroleum Engineer's R&D Competition at SPE Annual Technical Conference and Exhibition (2014). Technology developed in his lab was tested on the International Space Station in 2017. Prof. Bahadur has authored 57 journal articles (h-index of 25), 33 articles in conference proceedings, 1 book chapter, and has 5 patents issued or pending. His research has been featured on the cover of ASME's Mechanical Engineering magazine, cover of journals (*ACS Nano, Advanced Optical Materials*) and in R&D magazine. His research has been highlighted in international news media (NBC, Washington Post). He teaches courses in the areas of heat transfer and fluid mechanics.

• **Abstract** : Thermal challenges are becoming increasingly critical in the packaging of power electronics devices. While electronics and circuitry has progressed beyond silicon, encapsulation materials remain grounded in the silicon era. The first part of this talk summarizes recent progress on the development of high thermal conductivity dielectric polymeric nanocomposites. Polymeric materials with thermal conductivities exceeding 10 W/mK are commercially available, and several studies report thermal conductivities > 50 W/mK. However, high thermal conductivity alone is inadequate to characterize the suitability of an encapsulation material. Analysis of other thermal aspects (diffusivity, glass transition temperature, anisotropy), mechanical properties (thermal expansion, elastic modulus) and electrical properties is critical for holistic multifunctional assessment. This talk summarizes state-of-the-art materials and outlines gaps for future research to bridge the gap between materials science and applications. Next, we detail a study on machine learning (ML)-based predictive techniques, used in conjunction with a game-theoretic approach to predict the benefits of advanced materials on hotspot temperature reduction. Parametric steady-state and transient thermal simulations are conducted for a 1.2 kV/444 A Silicon Carbide (SiC) half-bridge module. The resulting databank of ~ 3800 data points is used to train and evaluate three ML algorithms (random forest, support vector regression and neural network) in modeling thermal behavior. The parameter space covers a variety of materials and cooling scenarios. Excellent prediction accuracies with R² values > 99.5% are obtained for the algorithms. Using ML-SHAP models, we quantify the impact of emerging polymeric nanocomposites on hotspot temperature reduction. Overall, we highlight the attractiveness of ML-based approaches for thermal design and provide a framework for setting targets for future encapsulation materials.

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The Evolution of High Temperature Pb-free Solder for Die-Attachment in Power Discrete Applications Sze Pei Lim, Indium Corporation

Speaker Bio: Sze Pei Lim is the Global Product Manager for Semiconductor and Advanced Materials , Indium corporation, Malaysia. She manages the semiconductor product lines globally and manages collaborates with external customers and corporate partners to support the industry's move towards heterogeneous integration. Some of her recent work includes the development of materials and processes for advanced packaging for fine feature printing for SiP application as well as for one-step OSP ball-attach applications. Sze Pei has more than 25 years of experience, specifically in the areas of PCB assembly and surface mount technology. She joined Indium Corporation in 2007 as a Technical Manager in Southeast Asia. Prior to that, she was a Research and Development Chemist, focusing on solder paste and flux formulation. Sze Pei also worked as a technical manager at Inventec for 9 years, where she provided technical support and managed testing in the lab. Sze Pei earned her bachelor's degree from the National University of Singapore, where she majored in industrial chemistry with a focus in polymers. She is a Certified SMT Process Engineer, has earned her Six Sigma Green Belt designation, and is heavily involved in many research and road mapping organizations.

Abstract: Development of high-temperature lead-free (HTLF) solders to replace high-lead solders for die-attachment in power device applications is driven by (1) the harmful effects of lead to human health and the environment, and (2) the demand of the improved bonding materials serving under high-power density and high-junction temperatures, especially for wide-band-gap power devices. A novel design, based on a mixed solder powder paste technology—Durafuse[™]—has been developed to deliver a Sn-rich HTLF paste, presenting the merits of both constituent powders. The combination of the rigid, high-melting SnSbCuAgX and the ductile, low-temperature Sn-rich solder in one paste enables reflow at a relatively low temperature (barely above the liquidus temperature of the final joint composition) and maintains the joint strength above 15MPa in the temperature range between 270°C and 295°C. The sufficient high-temperature strength has demonstrated the capability of maintaining the joint integrity during subsequent multiple SMT reflows below the 270°C peak temperature, regardless of the existence of a partial melting phase. Both X-ray inspection and cross-section microstructure have not shown any damage in the Si die or any noticeable cracks in the bonding joint, even after 3000 cycles of TCT (-40 to 150°C). In summary, Durafuse[™] HT, the novel design of the high-temperature lead-free pastes, has shown the feasibility as a drop-in solution to replace high-lead solders for die-attachment in power discrete applications

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Challenges and requirements for Seed Layer Deposition on Organic Substrates, Suresh Kumar Singaram, Evatec SEA

Speaker Bio: Dr Suresh has been in the semiconductor equipment business for 20 years holding various roles in engineering, product management, global technical support and operations. Dr Kumar currently heads a regional team in Evatec SEA which provides software support, advanced process development as well new platform/technology transfer from Evatec HQ into the region. Dr Kumar's current interests include the use of AI and machine learning for advanced analytics in process control as well as diagnostics. Dr Kumar holds a PhD in Plasma Physics from Nanyang Technological University Singapore.

Abstract: Fan out (FO) packaging is one of the key growth areas in advanced packaging. With high adoption rates and strong technology advantages it offers a strong pathway forward to support current industry roadmaps. Seed layer deposition is one of the most critical process steps in the manufacturing of vertical and horizontal interconnects. At both the wafer level and panel level, seed layer deposition must deposition must deliver high-performance degas, etch and sputter deposition processes whilst managing the substrate temperature throughout the whole process to ensure low contact resistance (Rc) and excellent adhesion of the seed layers prior to downstream processing. (lithography, electroplating etc.). In this presentation we will share the results from work done to achieve a superior seed layer performance while maintaining high throughput

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Technology and Market Briefing on Semiconductor Packaging, Favier Shoo, Yole Development

Speaker Bio: Favier Shoo is a Team Lead Analyst in the Packaging team within Semiconductor, Memory and Computing Division at Yole Développement (Yole), part of Yole Group of Companies. Based in Singapore, Favier manages an international team and develops the technical expertise and market know-how within the team. Favier generates technology & market reports, provides strategic consulting and performs custom studies. As an acknowledged professional in the semiconductor packaging marketspace, Favier is regularly engaged in international conferences, with presentations, keynotes, and panel review sessions. During 7 years at Applied Materials as a Customer Application Technologist in the advanced packaging field, Favier developed an in-depth understanding of the supply chain and core business values. Favier holds a Bachelor's in Materials Engineering (Hons) and a Minor in Entrepreneurship from Nanyang Technological University (NTU) Singapore. Favier was also the co-founder of a startup company where he formulated business goals, revenue models and marketing plans

Abstract : Fueled by digital end-system demands and technological innovation, Advanced Packaging technology options are increasingly rich and ground-breaking. Performance/power improvements at escalating cost associated with Moore's Law scaling had triggered semiconductor industry to strategize system-level scaling with Advanced Packaging solutions instead of purely scaling FE advanced nodes. The industry is now diligently using advanced packaging technologies to put multiple advanced and/or mature chips in a single package. Together with 3D packaging this extends Moore's Law at system-level. Times have changed. The total IC packaging market was worth \$68B in 2020. Advanced Packaging was worth \$30B and is expected to grow at CAGR₂₀₂₀₋₂₀₂₆ of 8% to reach \$48.2B in 2026. At the same time, traditional packaging market will grow at CAGR₂₀₂₀₋₂₀₂₆ of 4.3% and total packaging market will grow at CAGR₂₀₂₀₋₂₀₂₆ of 6% to \$47.9B and \$96.1B, respectively. Compared to traditional packaging which will grow at 3.2% CAGR₂₀₁₄₋₂₀₂₆, Advanced Packaging will grow more than 2 times quicker, with its CAGR₂₀₁₄₋₂₀₂₆ of 7.5%. Two Advanced Packaging roadmaps are foreseen – scaling (going to sub10 nm nodes) and functional (staying above 20nm nodes). The semiconductor manufacturing supply chain is undergoing change at various levels. In order to expand the business and explore new areas, players in semiconductor supply chains are moving to different business models. Among them, the most dynamic is the Advanced Packaging business

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Hybrid Two-Phase Cooling Technology for Next-Generation Datacenters, Raffaele Luca Amalfi Nokia Bell Labs New Jersey

Speaker Bio: Dr. Luca is a Senior Lead Researcher at Nokia Bell Labs New Jersey, where he performs cutting-edge research in the field of thermal management of high-performance communications and computing systems across multiple scales. Since 2016 he worked as Scientific Collaborator and Lab Operations Manager at the Swiss Federal Institute of Technology of Lausanne, at the Heat and Mass Transfer Lab, in Switzerland. In 2015 he joined Alcatel-Lucent in New Jersey, where he performed disruptive research on hybrid air/liquid cooling technologies for network equipment. In 2012 he joined IBM Research Lab in Switzerland, where he developed a novel cooling system for high-heat flux servers. Dr. Amalfi's research activities include macro-to-micro-scale heat and mass transfer, two-phase flow in complex structures, thermal-mechanical design of advanced heat exchangers, integrated opto-electronics thermal management, active and passive thermal technologies for electronics-, power-electronics- and datacenter-cooling. He has received a Ph.D. in Energy Engineering from the Swiss Federal Institute of Technology of Lausanne and authored over 40 scientific publications in leading journals, conference proceedings and handbooks. Dr. Amalfi is a Member of the ASME K-16 Heat Transfer Committee and Guest Editor for the ASME Journal of Electronic Packaging. He is the recipient of the Best Paper Runner-up Award at IEEE ITHERM 2021, Best Paper Award at IEEE ITHERM 2020 and Outstanding Paper Award at ASME InterPACK 2017

Abstract :Data processing, transport and storage demands are exponentially increasing, driven by applications in mobile broadband, video and gaming, cloud, 5G networks, Artificial Intelligence and Internet of Things. Such trends are directly linked to next-generation "digital transformation", which is dominated by intelligent machine-to-machine and human-to-machine communications, automating "everything everywhere" in a new ecosystem. This has profound implications in terms of overall system design with the associated general trend towards achieving greater system functionality per unit volume. In this talk, I will present a hybrid two-phase cooling technology that uses passive heat transfer devices to dissipate the heat generated by the high heat-generating components inside the servers. The heat is then transferred to compact heat exchanger condensers, which in turn dissipate the total heat from the racks into the room-level cooling loop. Air-cooling is still used for the low heat-generating components to make the technology cost effective. The thermal performance of the server-level passive heat transfer devices is extracted from experimental measurements, while air-cooling performance and flow distribution are investigated via computational simulations. Results shows that the proposed technology ensures enhanced cooling for all the hardware components and significantly reduces energy consumption, demonstrating its potential to scale existing hardware and build next-generation datacenters, while keeping low costs and being environmentally-friendly

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Material development enabling High-Speed and High-Frequency in Advanced Packaging Applications, Michael Gallagher, DuPont Electronics and Industrial

Speaker Bio: Michael is R&D Fellow in Semiconductor Technologies division of DuPont Electronics and Industrial. His primary responsibility is development of new polymeric materials and integration processes for Packaging and 3D-Interconnect Technologies. Prior to his current role, Michael led an R&D teams in Advanced Packaging developing photo-dielectric, bonding and underfills materials and in Semiconductor Technologies developing both lithographic materials and low-k dielectric materials. He joined the Rohm and Haas Company in Spring House, PA in 1987 and worked for Plaskon Electronic Materials developing novel EMCs used to package SMDs. In 2001, Michael transferred to the Shipley Company in Marlborough, MA to lead a team developing porous low K dielectric and air gap materials for semiconductor back-end processing. He has more than 60 granted patents as well as over 40 presentations and papers relating to electronic materials and their integration. He is a member of IEEE and serves on the Packaging Technologies committee for ECTC. Michael earned a B.S. in Chemistry from Yale University in New Haven, CT, a Ph.D. in Inorganic Chemistry from M.I.T in Cambridge, MA followed by postdoctoral research at the Technische Universität Berlin in Germany and at the M.I.T. Ceramics Processing Research Labs.

Abstract: Artificial Intelligence, Autonomous Driving, High Performance and Edge Computing 5G, IoT, smart connectivity and Quantum computing have increased the need for high data transfer rates and greater bandwidth which requires a multigenerational connectivity network over the next few decades. The ubiquitous demand for data and connectivity has created needs for materials with unique properties to deliver high performance in this expanding ecosystem. Designers faced with new demands arising from frequencies up to 100 Gigahertz and beyond are constrained by miniaturization, shorter development cycle times and need for cost effective solutions. Critical areas requiring new material innovations include high speed digital, high frequency applications, thermal management, shielding needs and power optimization. To meet these challenges, DuPont offers a wide range of customizable solutions including low loss dielectric resins and laminates, conductor metallurgies, ceramics, materials for heat dissipation and power optimization. Our solutions for high speed and high frequency systems are widely used in applications for mobile, radar, telecommunications, satellite technology, consumer, medical and a host of others where a high level of reliability, efficiency and performance are critical. Today we will discuss a few of our materials.

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Fan Out Packaging and its Diversity John Hunt, ASE

Speaker Bio: John Hunt is Senior Director Engineering, Marketing & Technical Promotion, at ASE (US) Inc., and provides technical support for the Introduction, Engineering, Marketing, and Business Development activities for Advanced Wafer Level and Fan Out Packaging Technologies at ASE. John has more than 45 years of experience in various areas of manufacturing, assembly and testing of electronic components and systems, with emphasis on the development of new technologies and processes. He has a B.S. from Rutgers and an M.S. from the University of Central Florida.

Abstract: Fan Out technology has evolved in recent years as an alternative package answering a growing need for miniaturization in electronics, while also providing improved electrical interconnectivity for more advanced multi-die solutions. This has been accomplished through the integration of a wide variety of wafer and panel level technologies, processes and materials. Fan out has enabled both the miniaturization of low-end packages for mobile applications, as well as the interconnection required for more advanced complex package assemblies. We will review these Fan Out technologies, including Wafer Level Fanout, Panel Level Fanout, and multiple combinations of chip first and chip last solutions. The resulting packaging combinations that evolve from these technologies will only be limited by our imaginations, and our creativity in innovating them.

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Augmented Finite Element Method (AFEM) for the Linear Steadystate Thermal and Thermomechanical Analysis of Heterogeneous Integration Architectures, Venkatesh Avula, Georgia Institute of Technology

Speaker Bio: Dr Avula received his B.Tech. degree in Electronics and Communication Engineering from Cochin University of Science and Technology (CUSAT), Kerala, India in 2004, and his 1 M.S. degree in Electrical Engineering from the University of Idaho, USA in 2016 respectively. Currently, he is pursuing his Ph.D. degree in Electrical and Computer Engineering at Georgia Institute of Technology. From 2004 to 2015 he worked in the areas of signal processing, signal integrity, and power integrity with various companies such as in DSP Audio, Tektronix, LSI logic, Avago technologies, and Seagate in Bangalore, India. Most recently, from 2017 to 2018, he was with Micron in Boise, USA as a package signal and power integrity engineer. He was awarded the Outstanding Master's Student Research and Creative Activity Award from the University of Idaho in 2017. He was also the recipient of the best poster award at the IEEE EDAPS conference in 2016, and was awarded the best overall poster, best paper runner-up and best poster awards in the mechanics and reliability track at the ITherm 2021. His current research interests include multi-physics design for heterogeneous integration, and signal and power integrity of digital systems. Avula is the Chair of the IEEE Electronics Packaging Society (EPS) student chapter at Georgia Tech.

Abstract : Heterogeneous integration offers electrical performance beyond-Moore's law and provides an opportunity for system scaling. These benefits however come at the cost of multi-physics design challenges. Thermo-mechanical stresses, for example, are accentuated with the dense integration of heterogeneous materials and cause reliability concerns and failures in the long run. Therefore, in the design stage, thermo-mechanical modeling and simulation is critical. The thermo-mechanical analysis is often performed under cyclic loading conditions either thermal or power cycling. The power-cycled analysis is more accurate and needs coupling between the thermal and mechanical domains. The coupling requirement calls for passing nodal temperature spatial prole from thermal domain to the mechanical domain at each time instant of the analysis and therefore poses computational complexity challenges to the traditional time-domain methods. In resolving these computational complexities, a novel frequency-domain method called augmented finite element method (AFEM) is presented. The proposed method considers the given cyclical computational problem as a periodic switched linear (PSL) system and is a linear extension of the harmonic balance FEM (HB-FEM). The method uses harmonic or spectral basis to black-box model the periodic time- varying behaviour of local finite elements and variables in the computational domain. Solving the augmented global stiffness matrix, assembled from the local elements, once directly gives the periodic time-varying solution, which is the nodal temperature and deformation response for the thermomechanical analysis. A test case, a glass embedded panel, is taken to verify the computational efficiency of the proposed method. The results show that the method addresses the time-scale and coupling challenges with the traditional time-domain multi-physics modelling and analysis.

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Plasma Dicing - a Key Enabler for Heterogenous Integration and Hybrid Bonding, Richard Barnett, SPTS

Speaker Bio: Richard Barnett, Director, Etch Product Management Richard Barnett is Director, Etch Product Management at SPTS, with over 20 years experience in a number of fields in the semiconductor industry. In 2007, he joined what was then Aviza Technology, becoming a part of the etch product management team utilising his background in DRIE processing to help achieve a market-leading install base for that technology. He is responsible for the management of SPTS' Mosaic plasma dicing product line and has written and presented many papers about this disruptive new approach to die singulation. Richard graduated from The University of Nottingham in the UK with a Bachelor's degree in Materials Engineering and Electronics before entering the semiconductor industry. His roles have bridged the various parts of the supply chain including fab process engineering, wafer supply, equipment vendor process engineer and product management.

Abstract : As early adopters of plasma dicing begin to expand production capacity and many more manufacturers begin to invest in this approach, plasma dicing systems need to be able to provide reliable solutions for high volume production across a number of device applications. Many benefits of plasma dicing have been widely promoted over the past few years, such as the release of wafer real estate and higher die strengths, and these are being applied in production for very small, mechanically fragile die and/or die which need high strength for long-term reliability in challenging operating environments, such as automotive applications. Now additional benefits of plasma dicing are being recognised for emerging hybrid bonding solutions being developed to replace copper microbumps in the search for even greater levels of integration. In hybrid bonding applications it is critical that the bonding surfaces all completely clean to ensure a reliable bond. It is the ability of plasma to singulate wafers in a much cleaner fashion, than mechanical saw or laser dicing, which is finding favour in the realm of hybrid bonding. This presentation will discuss this emerging application and give also an overview of the latest hardware developments, including the launch of a new high volume production platform with overhead transport capability, and a new etch module to manage any fluorine left behind by the silicon dicing process, as well as a general update on market and process trends.

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Addressing the Large Field Size Challenges for Small Liner/Space RDL Interposers, Jinho An, Applied Material

Since January 2021, Dr. Jinho An has been serving as an Account Technologist Director in the Advanced Packaging Business Unit of Applied Materials Inc. Before Applied, he worked for over 10 years as a process development engineer for Samsung's Semiconductor R&D Center and Package Development Team working on TSV and RDL process development. During this time, he was a technical leader in charge of the wafer-level process development including CVD, PVD, wet clean, Dry Etch, EP, CMP, and photolithography. Jinho An has a Ph.D. in Materials Science and Engineering from the University of Texas at Austin.

Abstract: Fan-out RDL is an advanced packaging platform that allows for heterogenous integration of multi-dies into a single package with higher I/O count and smaller form factor high-performance computing and mobile devices among others. While small liner/space fanout technology has already been widely developed for such high-end computing applications, it has yet to reach significant volume manufacturing. For applications that would require multiple HBMs, the extremely large RDL field sizes can especially pose many yield, cost and performance challenges that can increase its manufacturing costs. This presentation looks at some solutions including lithography, testing and PVD that may allow for cost-effective manufacturing of this key technology.

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