EPTC 2021 | Final Program | Live Sessions

Date	Singapore Time Begin	Singapore Time End	Duration (min)	Agenda	Presentation Topic	Presenter/	Affiliation
	Session Chair: Dr Toh Chin Hock, Singapore						
Dec 1 2021	8:45am	8:50am	5	Welcome Address	EPTC 2021 General Chair	Dr Tang Gongyue	Institute of Microelectronics, Singapore
	8:50am	9:00am	5	Opening Address	EPS President	Prof Chris Bailey	
	9:00am	10:00am	60	Keynote 1	Advanced Package Fab Solution for Next Generation Devices	Dr Seung Wook Yoon	Samsung Electronics, Korea
	10:00am	11:00am	60	Technology Talk	Roadmap based on Holistic Understanding of Thermo-mechanical Challenges from Package to System to Maximize Silicon Performance	Dr Gamal Refai-Ahmed	Xilinx, USA
	11:00am	12:00pm	60	Technology Talk	Innovative Copper Electrodeposition Solutions for High-Density Fanout Package Technology	Bryan Buckalew	Lam Research, USA
	Session Chair: Dr Chui King Jien, IME Singapore						
	2:30pm	3:30pm	60	Keynote 2	Future directions for 3D Integration technologies, enabling further electronic system-level scaling benefits	Dr Eric Beyne	IMEC, Belgium
	3:30pm	4:30pm	60	Technology Talk	Memory Packaging Trends	Emilie Jolivet	Yole Développement, France
	4:30pm	5:30pm	60	Technology Talk	Thermal Management challenges for Advance Packaging in HPC/AI/ML	Dr Andy C. Mackie	Indium, USA
	Session Chair: Srinivas Vempati, IME Singapore						
Dec 2 2021	9:00am	11:00am	120	EPTC Panel Forum	Supply Chain Ecosystem Challenges Impacting Global Electronic Packaging	Dr Kitty Pearsall (Moderator) Dr C. P. Hung (Panelist) Nelson Fan (Panelist) Jan Vardenman (Panelist)	BOSS PRECISION, INC ASE, USA ASM PT, HK TechSearch International, USA
	11:00pm	12:00pm	60	Technology Talk	Burn-in Testing (BIT) in Electronic Manufacturing: to BIT or not to BIT, this is the question	Prof Suhir Ephriam	Portland State University, USA
	Session Chair: Ranjan Rajoo, GlobalFoundries Singapore						
	3:00pm	4:00pm	60	Keynote 3	Packaging Materials as a Key Enabler for Future Megatrends	Dr Klemens Brunner	Heraeus Electronics, Germany
	4:00pm	5:00pm	60	Technology Talk	Hybrid Bonding – State-of-the-Art and Upcoming Requirements	Paul Lindner	EV Group, Austria
	Session Chair: Dr Tang Gongyue, IME Singapore						
Dec 3 2021	9:00am	11:00am	120	HIR Roadmap Workshop	Heterogeneous Integration Roadmap Workshop (HIR)	Dr Bill Chen (Moderator) Dr Ravi Mahajan (Panelist) Dr WR Bottoms (Panelist) Dr Patrick McCluskey (Panelist Dr Amr Helmy (Panelist)	ASE, USA Intel, USA Third Millennium Test Solutions University of Maryland University Toronto
	12:00pm	1:30pm	90	IEEE YP Event	IEEE Young Professionals Panel discussion	Liu Yan (Moderator) Adeel Bajwa (Co-moderator) Dr Kitty Pearsall (Panelist) Subramanian S. Lyer (Panelist)	Medtronic Kulicke & Soffa BOSS PRECISION, INC UCLA, USA
	Session Chair: Dr Chandra Bhesetti, IME SIngapore						
Dec 7 2021	9:00am	11:00am	120	Special Forum	Can companies benefit from AI in Smart Manufacturing environment?	Chan Pin CHONG (Moderator) Dan Gamoto (Panelist) Koen De Backer (Panelist) Ranjan Chatterjee (Panelist) Tick Kwang (TK) Loh (Panelist)	Kulicke & Soffa Jabil Micron Technology Inc Cimetric Inc Kulicke & Soffa

EPTC 2021 | Final Program | Invited Papers and PDC

Date	Duration (min)	Agenda	Presentation Topic	Presenter (Affiliation)
Dec 1 to Dec 31 2021	24h x 7d on-demand video	Invited Paper 1	Memory Integration Solution in Advanced Package	Yu Po Wang (SPIL, Taiwan)
		Invited Paper 2	Hybrid Bonding Technology for high density 2.5D and 3D IC Integration	Masaya Kawano (IME, Singapore)
		Invited Paper 3	STT-MRAM Product Reliability and Magnetic Package Shielding Designs to Improve Immunity to External Magnetic Field and RF Sources	Vinayak Bharat Naik (GlobalFoundries, Singapore)
		Invited Paper 4	Assessing the Impact of Novel Polymers and Thermal Management in a Power Electronics Module Using Machine Learning Approaches	Vaibhav Bahadur (The University of Texas, Austin)
		Invited Paper 5	The Evolution of High Temperature Pb-free Solder for Die-Attachment in Power Discrete Applications	Sze Pei Lim (Indium Corporation)
		Invited Paper 6	Challenges and requirements for Seed Layer Deposition on Organic Substrates	Suresh Kumar Singaram (Evatec SEA)
		Invited Paper 7	Technology and Market Briefing on Semiconductor Packaging	Favier Shoo (Yole Development, Singapore)
		Invited Paper 8	Hybrid Two-Phase Cooling Technology for Next-Generation Datacenters	Raffaele Luca Amalfi (Nokia Bell Labs, New Jersey)
		Invited Paper 9	Material development enabling High-Speed and High-Frequency in Advanced Packaging Applications	Michael Gallagher (DuPont Electronics and Industrial, USA)
		Invited Paper 10	Fan Out Packaging and its Diversity	John Hunt (ASE, USA)
		Invited Paper 11	Augmented Finite Element Method (AFEM) for the Linear Steady-state Thermal and Thermomechanical Analysis of Heterogeneous Integration Architectures	Venkatesh Avula (Georgia Institute of Technology, USA)
		Invited Paper 12	Plasma Dicing - a Key Enabler for Heterogeneous Integration and Hybrid Bonding	Richard Barnet (SPTS, UK)
		Invited Paper 13	Addressing the Large Field Size Challenges for Small Liner/Space RDL Interposers	Jinho An (Applied Materials, Korea)

Date	Duration (min)	Agenda	Presentation Topic	Presenter (Affiliation)
Dec 1 to Dec 31 2021	24h x 7d on-demand video	PDC 1	Antenna-in-Package (AiP) Technology for Millimeter-Wave Applications	Professor Y. P. Zhang (NTU, Singapore)
		PDC 2	Packaging and Heterogeneous Integration for Automotive Electronics, and Advanced Characterization of EMCs	Dr Przemyslaw Gromala (Robert Bosch, Germany)
		PDC 3	Fan-out, Chiplets and Hybrid Bonding	Dr John Lau (Unimicron, Taiwan)
		PDC 4	Flip Chip Interconnect Technologies	Dr Shengmin Wen (Synaptics, USA); Eric Perfecto (IBM, USA)
		PDC 5	ESD Impact and Risk on IC Package Technology Development and MEMs Devices	Dr Charvaka Duvvury

EPTC 2021 | Final Program | Technical Sessions

Date	Duration (min)	Technical Sessions	Paper ID	First Author	Affilication	Title
Dec 1 to Dec 31 2021	24h x 7d on-demand video	3D Integration & Hybrid Bonding 1	124	Yu, Zechun	Fraunhofer IISB, Germany	Cu-Cu Thermocompression Bonding with Cu-Nanowire Films for Power Semiconductor Die-Attach on DBC Substrates
		3D Integration & Hybrid Bonding 1	156	Hahn, Seung Ho	Mechatronics R&D Center, Samsung Electronics, South Korea	Atomistic-scale Simulations on Surface Activation Process of Dielectric Oxides for Hybrid Bonding Applications
		3D Integration & Hybrid Bonding 1	183	Wai, Leong Ching	Institue of Microelectronics, Singapore	Realization of High Aspect Ratio Through Mold Interconnect (TMI) using Vertical Wire
		3D Integration & Hybrid Bonding 1	211	Seit, Wen Wei	Institute of Microelectronics, Singapore	Comprehensive Study on Polymer Based Chip-to/chip Bonding For Gas Sensor Application
		3D Integration & Hybrid Bonding 2	194	Choi, Won Young	Samsung Electronics, Korea, Republic of (South Korea)	Characteristics of Plasma Treated Surface for SiO2-Si Wafer Bonding
		3D Integration & Hybrid Bonding 2	212	JI, Hongmiao	Institute of Microelectronics (IME), A*STAR, Singapore	Cu CMP Dishing in High Density Cu Pad for Fine Pitch Wafer-to-Wafer (W2W) Hybrid Bonding
		3D Integration & Hybrid Bonding 2	223	Li, Hongyu	IME, Singapore	Wafer-to-Wafer Hybrid Bonding Challenges for 3D IC Applications
		3D Integration & Hybrid Bonding 2	235	Bhuvanendran, Say	Institute of Microelectronics (IME), A*STAR, Singapore	Towards Heterogeneous Integrated Electronic-Photonic Packages for Hyperscale Data Centers
		3D Integration & Hybrid Bonding 2	243	Viklund, Per	Siemens EDA, United States of America	Successful heterogeneous integration of chiplet's demands “shift-left” system level optimization
		Advanced FA and Reliability 1	102	Tan, Rui Zhen	Singapore Institute of Technology, Singapore	Localization of Hotspots from Lock-in Thermography Images for Failure Analysis
		Advanced FA and Reliability 1	103	Hua, Younan	WinTech Nano-Technology Services Pte. Ltd., Singapore	Failure Analysis & Mechanism Studies of the Worm-like Defects in Vias of Wafer Fabrication
		Advanced FA and Reliability 1	104	Hua, Younan	WinTech Nano-Technology Services Pte. Ltd., Singapore	Failure Analysis and Elimination of the Bromine-induced Defects in Wafer Fabrication
		Advanced FA and Reliability 1	107	Ha, Job	samsung electronics, Korea, Republic of (South Korea)	Photo-resist Residues and Electrochemical Migration Failure under Biased HAST
		Advanced FA and Reliability 2	116	Arellano, Ian Harvey	STMicroelectronics, Inc., Philippines	Foreign Materials Management: A Critical but Overlooked Element in Optoelectronic Device Introduction
		Advanced FA and Reliability 2	181	Buenviaje Jr., Salvador Cruz	STMicroelectronics, Inc., Philippines	Understanding Sulfur-Induced Surface Discoloration of QFN-mr Leads After Prolonged Environmental Exposure
		Advanced FA and Reliability 2	215	Che, Faxing	Micron Semiconductor Asia Operations Pte. Ltd, Singapore	Failure Mechanism and Prevention of Die Cracking for FBGA Package Misplaced in the Tray
		Advanced FA and Reliability 2	254	Viswanathan, Vignesh	ZEISS, Singapore	Developments in Advanced Packaging Failure Analysis using Correlated X-Ray Microscopy and LaserFIB
		Advanced FA and Reliability 2	255	Stoynova, Anna	Technical University of Sofia	Non-destructive thermal diagnostics of multilayer substrates for multichip modules
		Advanced Inspection and Metrology	128	Ke, Chung-Yu	Siliconware Precision Industries Co., Ltd., Taiwan	2D X-Ray Void Detection for Next Generation Copper Pillar Bump
		Advanced Inspection and Metrology	129	Ke, Chung-Yu	Siliconware Precision Industries Co., Ltd., Taiwan	X-ray inspection for FOMCM (Fan-Out Multi Chip Module)
		Advanced Inspection and Metrology	219	Chen, Hu	Key Laboratory of Advanced Display and System Application, China	Direct X-Ray Detectors Based on polydimethylsiloxane
		Advanced Inspection and Metrology	220	Xue, Feng	IBM, Singapore	iNEMI Organic Panel and Laminate Fine Circuit Pattern Inspection and Metrology HVM Readiness
		Advanced Inspection and Metrology	242	Kho, Kok Tai	Qualcomm Global Trading Pte. Ltd. Singapore	Detecting Wire Bond Inter Layer Dielectric Crack by Dark Field Imaging
		Assembly Equipment and Process Designs	125	Hendi, Ihssan	CEA Tech, France	Electrical functionalisation by additive manufacturing
		Assembly Equipment and Process Designs	250	Géczy, Attila	Budapest University of Technology and Economics, Hungary	Flow and Gauge Sensor Fusion in Vapour Phase Soldering Ovens for Optimized Process Control
		Assembly Equipment and Process Designs	257	Loh, Tick Kwang	Kulicke & Soffa Pte Ltd, Singapore	Kulicke & Soffa: Enabling predictive analytic through deep learning
		Assembly Materials and Processing 1	114	Wang, Miao (1)	NXP Semiconductors	Intermetallic growth and void formation mechanism in flip chip copper pillar interconnects: role of the underfill material
		Assembly Materials and Processing 1	121	Teng, Wen-Yu	Siliconware Precision Industries Co., Ltd., Taiwan	Advanced Thermal Lid Attach Adhesive for High Performance Computing (HPC) Package
		Assembly Materials and Processing 1	131	Salam, Budiman	Singapore Institute of Manufacturing Technology, Singapore	Dispensing Process of Silver Adhesive to Minimize the Joint Surface Area-to-Volume Ratio for Premature Dried Adhesives Prevention
		Assembly Materials and Processing 1	145	Nantes, Donald	Heraeus Materials Singapore Pte Ltd, Singapore	Fine Pitch Microdots Dispensing and Jetting Optimization in SiP Assembly using Welco Solder Paste
		Assembly Materials and Processing 1	153	Hu, Liangxing	Nanyang Technological University, Singapore 639798	Systematic Investigation and Characterization of Ag Paste for LED Die Attach
		Assembly Materials and Processing 1	256	Zhu, Xintong	GLOBALFOUNDRIES Singapore Pte Ltd	Dicing Blade Characterization Using Nano-indentation
		Assembly Materials and Processing 2	172	Lo, Shih Kun	ASECL, Taiwan	Investigation of the flow behaviors for capillary underfill process in flip chip packaging
		Assembly Materials and Processing 2	179	Li, Zhiwen (1)	Nexperia, Hong Kong	Die Attach Material Optimization for Enhancing Package Integrity of Surface Mount Device after Moisture Sensitivity Level 1
		Assembly Materials and Processing 2	193	Xi, Chengjie	University of Florida, United States of America	Microelectronic Encapsulant Material Assessment: A Security Point of View
		Assembly Materials and Processing 2	233	Delos Santos, Dexter	STMicroelectronics, Philippines	Effect of Moisture in a Non-conductive Glue on the Electrical Performance of a Cavity Package
		Assembly Materials and Processing 2	236	Chen, Felix C.	Kymeta Corporation, United States of America	Acceleration Factor For Polymer Degradation by UV Light Exposure
		Assembly Materials and Processing 2	251	Horiki, Eita	Sekisui Chemical Co., Ltd., Japan	Development of Build-up Dielectric Material that enables High Temp. Low Loss, High Fracture Toughness Advanced FC-BGA Substrates
		Emerging Technologies 1	106	Takehana, Mark	University of California, Irvine, United States of America	Investigation of Thermoelectric Cooling for a Competition Electric Vehicle
		Emerging Technologies 1	110	Elgndi, Bishoy	Queens University, Canada	Polarization-Insensitive Metalenses at Wavelengths in Ultraviolet Region
		Emerging Technologies 1	118	Li, Jinming	Huazhong University of Science and Technology, China	Molecular dynamics study of BNNS/Al composites under compression
		Emerging Technologies 1	166	Lee, Chu-Chung Stephen	NXP semiconductor, United States of America	MAXQFP: NXP new package platform
		Emerging Technologies 2	130	sunappan, vasudivan	Singapore Institute of Manufacturing Technology, Singapore	Parametric Study of Gravure Printing for Electric Heaters
		Emerging Technologies 2	216	Sikkandhar, Musafargani	Institute of Microelectronics, A*STAR, Singapore	Reference Free Ion-Selective Electrode for sensing Potassium Ions
		Emerging Technologies 2	241	Wang, Ke	Institute of Microelectronics, China	Degradation of SOI SRAMs at 250°C operating conditions

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Date	Duration (min)	Technical Sessions	Paper ID	First Author	Affilication	Title
Dec 1 to Dec 31 2021	24h x 7d on-demand video	Fan-Out Processes and Processing 1	147	Yu, Yeonseop	Samsung Electronics, Korea, Republic of (South Korea)	Diffusion and oxidation of copper in polymer of Fan Out-Panel Level Package (FO-PLP) under High Temperature Storage (HTS) Conditions
		Fan-Out Processes and Processing 1	149	Lin, Yu Ting	ASE Group, Taiwan	Investigation on the reliability risk for high density Fan-Out packages
		Fan-Out Processes and Processing 1	151	Liu, Shuai-Lin	SPIL, Taiwan	Fan-Out Embedded Bridge Solution in HPC Application
		Fan-Out Processes and Processing 1	155	Lau, Boon Long	IME Astar, Singapore	Fabrication Process Flow of Antenna-in-Package Fan-out Wafer Level Packaging
		Fan-Out Processes and Processing 1	248	Jhong, Ming-Fong	ASE, Taiwan	Hybrid RDL Design in Fan-out Package
		Fan-Out Processes and Processing 2	168	Sun, Mei	Institute of Microelectronics, Singapore	Dual Polarized FOWLP AiP for 5G Base Station Applications
		Fan-Out Processes and Processing 2	178	Li, Jay	SPIL, Taiwan	Large Size Multilayered Fan-Out RDL Packaging for Heterogeneous Integration
		Fan-Out Processes and Processing 2	198	Zhang, Shuye	Harbin Institute of Technology, China, People's Republic of	Shear Performance and Accelerated Reliability of 6 x 6 mm2 FOWLP Solder Joints using an ENIG based PCB Electrode
		Fan-Out Processes and Processing 2	204	Chai, Tai Chong	IME, Singapore	Heterogeneous Integration on Fan-Out Wafer Level Packaging Plat Form
		Fan-Out Processes and Processing 2	210	Hsiao, Hsiang Yao	Institute of Microelectronics, Singapore	Through Mold Via Development Using Laser Drilling Process for 3D Fan-out Wafer Level Package
		Fan-Out Processes and Processing 2	240	Sandstrom, Clifford	Deca Technologies, United States of America	Deca & ASE Scaling M-Series & Adaptive Patterning to 600mm
		Leadframe & Substrated Based Packages	120	Talledo, Jefferson Sismundo	STMicroelectronics, Philippines	Development of an Innovative Leadframe Design for Eliminating Lead Delamination
		Leadframe & Substrated Based Packages	163	Pun Po Leung, Kelvin	Compass Technology Company Limited, Hong Kong S.A.R. (China)	Flexible Integrated Battery on System-in-Package (SiP) for Internet of Things (IoT) and Smart Wearables
		Leadframe & Substrated Based Packages	174	Pulutan, Marty Lorgino	Ampleon Philippines Inc, Philippines	Surface Plasma and Mold Deflash Treatment of Plated and Non-Plated Cu Leadframe for Leadframe-to-Mold Adhesion Improvement
		Leadframe & Substrated Based Packages	190	Serapio, Listangco	STMicroelectronics, Inc., Philippines	Determination of Optimal Setting for the Tape-Based Partial Package Sawing of Wettable Flank QFN Package
		Leadframe & Substrated Based Packages	213	Lim, Ruiqi	Institute of Microelectronics, Singapore	Pressure Sensor Substrate for Prolonged Sitting and Posture Monitoring
		Power Packages and Sintering	138	Hadeler, Steffen	1: Institute of Micro Production Technology, Garbsen, Germany	Investigations on Silver Sintering using an Ultrasonic Transient Liquid Phase Sintering Process
		Power Packages and Sintering	171	Obed Jr., Rommel Santiago	Ampleon Philippines Inc., Philippines	Effect of Nickel, Silver, and Gold Wafer Backside Metallization (BSM) on 80Au20Sn (Gold-Tin) Die Attach
		Power Packages and Sintering	176	Li, Jinyuan	Key Laboratory of Advanced Power Transmission Technology, China	Study on the Impacts of Clamping Process Defects to the Reliability of Press-Pack IGBTs
		Power Packages and Sintering	209	Yang, Hui	Guilin university of technology	Progress on low temperature sintering of nano-silver
		Power Packages and Sintering	234	Ma, Chuangwei	Central South University, China, People's Republic of	Comparison of Embedded Packaging Versus Traditional Packaging of GaN HEMTs on High Frequency Performance in Half-Bridge Circuits
		Power Packages and Sintering	239	Zhu, Jiaqi (1)	Northwestern Polytechnical University	Porosity effect on fracture behaviour of sintered silver nanoparticles by phase-field modelling
		RF, 5G and mmWave Packaging 1	133	Yamamoto, Shuya	Kyushu University, Japan	High Efficient RF Energy Harvesting Circuit using Cascade Structure
		RF, 5G and mmWave Packaging 1	134	Tasaki, Kohei	Kyushu University, Japan	Terahertz band on-chip one-sided directional wide band slot array antenna
		RF, 5G and mmWave Packaging 1	135	Yamamoto, Shunsuke	Kyushu University, Japan	One-sided directional slot array antenna for 28GHz wideband operation
		RF, 5G and mmWave Packaging 1	137	Tsai, Mike	SPIL, Taiwan	Alternative Low Cost EMI Shielding Solutions of SiP Module for 5G mmWave Applications
		RF, 5G and mmWave Packaging 2	169	Fujii, Yuki	Kyushu University, Japan	Development of a wide-band compact diplexer using a redistribution layer for 5G application
		RF, 5G and mmWave Packaging 2	188	Wu, Jiaqi	Institute of Microelectronics, A*STAR, Singapore	RF Performance Study of Through-Mold-Via (TMV) using L-2L De-Embedding Method
		RF, 5G and mmWave Packaging 2	199	Chong, Ser Choong	Institute of Microelectronics, Singapore	Assembly and Packaging of Miniature Nanoantenna Spatial Light Modulator
		RF, 5G and mmWave Packaging 2	203	Lim, Sharon Pei Siang	Institute of Microelectronics, Singapore	Addressing the assembly challenges of Antenna-in-package
		RF, 5G and mmWave Packaging 2	225	Chippalkatti, Vinod	Centum Electronics Limited Bangalore, India	High density packaging techniques for miniaturization of satellite RF and microwave subsystems
		Signal Integrity & Power Integrity Design 1	148	LIU, xuena	Academy of Smart IC and Networks, China	An Effective Coding Transmission Scheme for TSV Array Transmission with Defects
		Signal Integrity & Power Integrity Design 1	157	Li, Kangrong	Institute of Microelectronics, Singapore	Systematic Signal Integrity Analysis on Fine Pitch Probe Card for HBM Interposer Testing
		Signal Integrity & Power Integrity Design 1	158	TANG, Qingyuan	Nexperia Hong Kong, Hong Kong S.A.R. (China)	Die Attach Effect on Electrical Performance and Reliability of Embedded Die Package
		Signal Integrity & Power Integrity Design 1	164	Zhang, Hengshuang	China Academy of Space Technology (Xi'an), China	Design and Implementation of a Ka-Ku Frequency Conversion Receiver 3D SiP Module
		Signal Integrity & Power Integrity Design 1	228	K R, SURESHA	Centum electronics Pvt ltd, India	Evaluation of Contact Conductance and Its Importance in Electronic Packaging
		Signal Integrity & Power Integrity Design 2	182	XU, Zhaoxin	Guangdong University of Technology, Guangzhou, China	Signal integrity analysis of butterfly-shaped vias for RF packages
		Signal Integrity & Power Integrity Design 2	191	Heinig, Andy	Fraunhofer IIS/EAS, Germany	A generic approach for automatic design rule derivation for assembly design kits (ADK)
		Signal Integrity & Power Integrity Design 2	192	Ahmed, Maudood	Fraunhofer Institute, Germany	Bunch of Wires Interface PHY Design for Multi-Chiplet Systems
		Signal Integrity & Power Integrity Design 2	195	Ress, Sandor	BME	On the Correction of the Effects of Electrical transients in the Measured Thermal Transients
		Signal Integrity & Power Integrity Design 2	200	Umralkar, Ratan	A*STAR, Singapore	Testing Multiple High Speed Channels using Automated Test Equipment(ATE), SOC 93K, in parallel
		Signal Integrity & Power Integrity Design 2	231	Lan, Jingjing	Institute of Microelectronics, Singapore	Chiplet-based Architecture Design for Multi-Core Neuromorphic Processor
		Solder Joint Characterization & Processing 1	117	Sinha, Koustav	Micron Technology, Inc., United States of America	Influence of BGA Design Parameters on Solder Joint Reliability
		Solder Joint Characterization & Processing 1	122	Zou, Yung-Sheng	Micron, Taiwan	Effects of Sb and Bi addition on IMC morphology and reliability of Pb-free solder/Cu-OSP
		Solder Joint Characterization & Processing 1	126	CHEN, CHIEN MING	Micron Technology, Inc.	Low Temperature Solder Paste Characterization during Memory Module and SSD Product Level Reliability Test
		Solder Joint Characterization & Processing 1	127	Liu, Vance (1);	Micron Technology, Taiwan	Comparative Study of Solder Strength Characterization for BGA Packages
		Solder Joint Characterization & Processing 2	150	Jaafar, Norhanani	Institute Of Microelectronic, Singapore	Comprehensive Study on Thermal Aging and Ball Shear Characterization of SAC-X Solders
		Solder Joint Characterization & Processing 2	154	Lee, Aaron	Advanced Micro Devices, Singapore	Application of EBSD Study of Cu-Sn IMCs in SAC305 and Sn0.7Cu Solder Joints
		Solder Joint Characterization & Processing 2	160	Lim, Michael Joo Zhong	Infineon Technologies Asia Pacific, Singapore	Copper wire degradation under high temperature and high humidity without molding compound
		Solder Joint Characterization & Processing 2	162	Su, Huan Ping	Ableprint Technology Co. Ltd., Taiwan	Effect of Pneumatic Reflow Profiling on Voiding Reduction in High-Lead Solder Die Attach

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Dec 1 to Dec 31 2021	24h x 7d on-demand video	Solder Joint Characterization & Processing 3	165	Chen, Yi	Loughborough University, United Kingdom	Interfacial reaction and mechanical properties of Cu/Ga/Cu interconnects during the transient liquid phase bonding
		Solder Joint Characterization & Processing 3	202	Zhang, Shuye	Harbin Institute of Technology, Harbin 150001, China	Effects of Co on the Morphology, Shear Strength and Fracture of the Low temperature SAC305/Sn-58Bi/Cu Composite Solder Joint
		Solder Joint Characterization & Processing 3	230	Xu, Junmeng	Northwestern Polytechnical University, Xi'an, China	Growth kinetics of intermetallic compound in solder joints during thermal cycling: a review.
		Solder Joint Characterization & Processing 3	238	xie, shuang	Beijing Microelectronics Technology Institute, China	Study on Mechanical Behavior and Long-term Storage Reliability of Micron-level Mixed Solder Joints
		Thermal Simulation and Characterization 1	105	Göktepe, Emine	Boğaziçi University, Turkey	Current Crowding Effects on the Thermal Performance of AlGaN/GaN Light Emitting Diodes
		Thermal Simulation and Characterization 1	112	Kim, JungKyun	Siemens EDA, Korea, Republic of (South Korea)	Thermal characterization of automotive power module with SHERPA
		Thermal Simulation and Characterization 1	113	Stoukatch, Serguei	Liege University, Belgium	Non-contact thermal characterization using IR camera for compact metal-oxide gas sensor
		Thermal Simulation and Characterization 1	143	Goswami, Avijit	Boyd Corporation, India	Thermal characterization of battery cold plates
		Thermal Simulation and Characterization 2	146	Du, Jianyu (1,2)	niversity of Geosciences, Beijing, China	Embedded Cooling for High Heat Flux Hot Spots in Different Sizes
		Thermal Simulation and Characterization 2	180	Pujahari, Ankita	IIT Kharagpur, India	Analysis of Evaporation from micropillar surface by Using Non-Uniform Heat Flux
		Thermal Simulation and Characterization 2	205	Han, Yong	Institute of Microelectronics, A*STAR, Singapore	Thermal effect investigation of chip-to-wafer hybrid bonding on 3D-stacked memory
		Thermal Simulation and Characterization 2	214	TANG, GONG YUE	Institute of Microelectronics, Singapore	Thermal design and analysis for double side cooling 6-in-1 SiC power module
		Thermal Simulation and Characterization 3	218	Chen, Haoran	Institute of Microelectronics, A*STAR research entities, Singapore	Numerical investigation of the optimization on manifold microchannel heat sink towards the water-cooling limit
		Thermal Simulation and Characterization 3	232	Thaher, Ahmed	United Arab Emirates University, UAE	Heat Sink Employing Straight Microchannels with Sidewall Ribs in Staggered Arrangement for Liquid Based Cooling of Microelectronic Chips
		Thermal Simulation and Characterization 3	246	Wang, Shizhao	Wuhan University, China	Numerical Model for Understanding Interconnection Thermal Reliability Mechanism of Cu Via in Back End of Line (BEOL)
		Thermo-mechanical Sim & Characterization 1	100	Refai-Ahmed, Gamal	Xilinx	Roadmap Based on Holistic Understanding of Thermo-Mechanical Challenges from Package to System to Maximize Silicon Performance
		Thermo-mechanical Sim & Characterization 1	101	Lee, C.L. Alan	Institute of Microelectronics, Singapore	Nonlinear Thermal Stress/Strain Analyses of Through SiC Via
		Thermo-mechanical Sim & Characterization 1	111	Yu, Wei (1)	Micron Semiconductor Asia Operations Pte. Singapore	Package Warpage Modeling by Considering Shrinkage Behavior of EMC and Substrate
		Thermo-mechanical Sim & Characterization 1	123	Sala, Simone Antonio	STMicroelectronics	Simulation of Moisture Ingression in Microelectronics Package to Correlate Tests and Field Conditions
		Thermo-mechanical Sim & Characterization 2	139	Matsuura, Masamitsu	Kyushu University, Japan	Study of Laser Ablation Slits in Stress Reduced Embedded Die Substrate Fabricated for Heterogeneous Integration
		Thermo-mechanical Sim & Characterization 2	141	Tippabhotla, Sasi Kumar	Institute of Microelectronics, Singapore	A comparative study of stress-based and fracture mechanics-based finite element simulation approaches for RDL based wafer level package
		Thermo-mechanical Sim & Characterization 2	142	Ji, Lin	Institute of Microelectronics Singapore	Numerical study on wafer level warpage evolution during chip to wafer hybrid bonding process
		Thermo-mechanical Sim & Characterization 2	161	Muller, Charles (1)	Murata Integrated Passive Solutions, SAS, Caen, France	Mechanical Robustness study of Ultra Low profile 3D Silicon capacitors
		Thermo-mechanical Sim & Characterization 2	196	Albrecht, Jan (1)	Fraunhofer Institute for Electronic Nanosystems ENAS, Chemnitz	Determining adhesion of critical interfaces in microelectronics – a Reverse Finite Element Modelling approach based on nanoindentation –
		Thermo-mechanical Sim & Characterization 3	217	Mandal, Rathin	Institute of Microelectronics, Singapore	Mechanical modeling study for fan-out wafer level package parameters to enhance BGA TCoB life
		Thermo-mechanical Sim & Characterization 3	222	BK, Chandrashekar	Centum Electronics limited, India	Thermo-Mechanical load Influence on Electronics Packages
		Thermo-mechanical Sim & Characterization 3	224	Baloglu, Eyup Can	Aselsan Inc, Turkey	The Effect of Adhesive and Carrier Material Properties on Thermo-Mechanical Stresses of GaSb, InSb Semiconductors due to Cryocooling
		Thermo-mechanical Sim & Characterization 3	227	Pulutan, Marty Lorgino	Ampleon Philippines Inc., Philippines	Design Selection and Optimization of Mechanical Anchoring Structure on Pre-plated Cu Leadframes
		Thermo-mechanical Sim & Characterization 3	229	Long, Xu	School of Mechanics, Northwestern Polytechnical University	Fatigue behaviour of small-sized in-situ packaging materials based on a single-point nanoindentation with cycle penetrations
		Thermo-mechanical Sim & Characterization 3	245	Jia, Qipu	School of Mechanics, Northwestern Polytechnical University	Determining mechanical properties of thin film in packaging structures by in-situ nanoindentation
		WLCSP, TSV and MEMS Processing 1	119	LIN, HSINJOU	Siliconware Precision Industries, Taiwan	High Reliability Solution of 2.5D Package Technologies
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		WLCSP, TSV and MEMS Processing 1	144	Zhao, Peng	Institute of Microelectronics, A*STAR, Singapore	Heating Dissipation Discussion of TSV-integrated Ion Trap with Glass Interposer
		WLCSP, TSV and MEMS Processing 1	152	Hwang, Gilho	Institute of Microelectronics, Singapore	Development of Metallization Process for Fine Pitch TSV
		WLCSP, TSV and MEMS Processing 2	207	Soh, Serine (1)	Institute of Microelectronics, Singapore	Low Temperature Oxide Passivation for Via-last/backside process
		WLCSP, TSV and MEMS Processing 2	208	Ho, Soon Wee David	Institute of Microelectronics, A*STAR, Singapore	High Density Redistribution Layers (< 2 um L/S) for Chiplets Packaging
		WLCSP, TSV and MEMS Processing 2	221	Loh, Woon Leng	Institute of Microelectronics, Singapore	A 2.5D Heterogeneous Integration Demonstration for High Performance RF Application using High-Resistivity Through Si Interposer (TSI)
		WLCSP, TSV and MEMS Processing 2	244	Benoit, Robert	DEVCOM Army Research Lab, United States of America	Effect of Via Placement on Wafer-Level Packaged Resonant MEMS Structures
		WLCSP, TSV and MEMS Processing 3	159	Komasu, Yuichiro	Lintec Singapore Pte. Ltd.	Development of UV Curable Wafer Back Side Protection-Film for Wafer Level Chip Size Package
		WLCSP, TSV and MEMS Processing 3	167	Wang, Xiangyu	Institute of microelectronics, Singapore	Silicon Isolation Trench Integration for the 4-stack Memory Wafer
		WLCSP, TSV and MEMS Processing 3	201	Shin, YongChul	Samsung Electronics, Korea, Republic of (South Korea)	Thin Wafer De-bonding for 3D-TSV Packaging of High Bandwidth Memory Devices using UV Irradiation
		WLCSP, TSV and MEMS Processing 3	206	Chockanathan, kanna	Institute of microelectronics, Singapore	SAW Cavity Sealing using Dielectric film in Wafer-level packaging