DEC 8, 2022 (Thursday)

	Veranda I	Veranda II	Veranda III	Riverfront I	Riverfront II	Riverfront III
Session Chair	Chul King Jen, Institute of Microelectronics	Albert Lan, Applied Materials	SB Park, The State University of New York	Roseanne Duce, STMicroelctronic	Bruce Kim, City University of New York	Changqing LIU, Loughborough University
08:30am -9:50am	A1: 2.5D, 3D and WL Packaging	A2: Hybrid Bonding Processes and Materials 1	A3: Wafer Level Processing I	A4: Leadframe and Subsrate Manufacturing I	A5: Electrical Simulations & Characterizations I	A6: Soldered and Sintered Interconnections I
8:30am - 8:50am	**A1.1 Stress-Free Thin-Die-Level De-bonding for 2.5D, 3DIC Packaging**	**A2.1 Numerical Simulations to Assist Chip-to-Wafer Hybrid Bonding Process Development**	**A3.1 Novel "Rigid Carrier with Composite Release Layer" to Assemble Ultra-High Density Advanced Packages & Substrates**	**A4.1 Analysis of leadframe discolouration on rough pre-plated frames (PPF) in wedbus packages**	**A5.1 Simulation Study of Newly Developed Magnetic Material for EMI Shielding on Solar Transformer**	**A6.1 Non-Pressure Ag-Sinter Bleed Out**
	Shin, YongChul; Kang, Suje; Park, Sun-Woo; Hong, Nung-Pyo; Lim, Kyungbin; Rhee, Minsoo	Tippabhotla, Sai Kumar; Ji, Lin; Chong, Ser Choong	Sohn, Hyun Bok; Nakazaki, Yoshihiro; Fuji Jiji; Kusakari, Kazuhiro; Yoshida, Takuya; Kuniyoshi, Shiho; Nakamura, Toshiki; Tanaka, Tatsuya; Okuyama, Kazuhiro; Kitabatake, Yukiko; Ishii, Reiko; Sayama, Motoyuki; Kobayashi, Kunihiro; Takaoka	Chan, Chun Ning (1); Gopalakrishnan, Purendran Ali. (2); Sekaran, Sreetharan Ali. (2); Li, Zhiwen (1)	Masuda, Seiya; Ohtsu, Akihiko; Miyata, Tetsushi; Suzuki, Hiroyuki; Takahashi, Hideroh	Long, Aubley;Pang, HuiShyan; Sanangapani, Murali; Balasubramanian, Senthil Kumar; Kang, SungSig
	Samsung Electronics, Korea	Institute of Microelectronics, A*Star Research Entities, Singapore	Mitsui Mining and Co., Ltd., Japan	Nexperia Hong Kong Limited, Hong Kong S.A.R. (China); Nexperia Malaysia Sdn Bhd Negeri Sembilan, Malaysia	FUJITSU Corporation, Japan	Heraeus Materials Singapore Pte. Ltd., Singapore
8:50am - 9:10am	**A1.2 Wafer Level Fabrication of CMUT using Bonding and Interconnection Technique without TSV/TSV**	**A2.2 Molecular Dynamics Study on Plasma-Surface Interactions of SiCN Dielectrics for Wafer-to-Wafer Hybrid Bonding Process**	**A3.2 Tunnable Profile with High Etch Rate Plasma Etching for 20% Scandium Doped Aluminium Nitride Film**	**A4.2 The Effect of Mixed Gas Ar+H2 Strip Plasma onto the Non-Roughened and Oxidation-Roughened Bare Cu Leadframe Surfaces**	**A5.2 From SI, PI, EMI Design, Verification, to Package, Board, and Channel Intellectual Property**	**A6.2 Temperature Cycling Performance of Bi-doped Solder Ball Alloy on DRAM Module Form and Daisy-Chained Printed Circuit Board**
	Adib, Adib (1); Agarwal, Rishabh (1); Sharma, Rishi (1); Maiolo, Luca (2); Minotti, Antonio (2); Maida, Francesco (2); Muntoiya, Ravindra (1)	Hahn, Seung Ho; Kim, Woojoung; Shin, Donggau; Lee, Yongin; Choi, Wonyoung; Moon, Bumki; Lim, Kyeongbin; Rhee, Minsoo	Suek, Zhan Jiang; Lin, Huanao; Tseng, Yat Fung; Rao, B S.S. Chandra	Pulusan, Marty Lorgino Dilaunan; Fernandez, Mathew Mondala; Estolano, Janice	Chen, Nensen	Zou, Yung-Sheng; Chung, M. H.; Chen, Jeremy; Gan, C.L.; Hsu, Claire; Tekiar, Hem
	CSIR-Central Electronics Engineering Research Institute, India; Institute for Microelectronics and Microsystems (IMM)-CNR, Italy	Samsung Electronics, Korea	Institute of Microelectronics, Singapore	Amphenol Philippines Inc., Philippines	MediaTek Inc., Taiwan	Micron Technology, Inc.
9:10am - 9:30am	**A1.3 Novel CMP material solution to enable high removal rate dielectric CMP for hybrid bonding application**	**A2.3 Evaluation of Polymer Materials for Hybrid Bonding Application**	**A3.3 Chemical-Mechanical Polishing of N-polar GaN for GaN HEMT on Diamond Bonding**	**A4.3 High performance multi-chip leadframe package with internal connection**	**A5.3 Low Power ALU Design with Incorporation of MWCNTB On-chip Interconnects**	**A6.3 Mechanical properties of transient liquid phase bonded joints by using Ag-In sandwich structure**
	Chakraborty, Tapas; Vethaverkatte, Steven; Chen, Han-Wen; Chandran, Gopi	Mishra, Dileep K; Vasarla, Nagendra Sekhar; Chong, Ser Choong; Vempati, Srinivasa Rao	Ranjan, Akhil (1); Lingapanthi, Ravikiran (2); Dharmarasu, Nethaji (2); Radhakrishnan, K (2)	Ankor technology, Korea, Republic of (South Korea)	Patabide, Takshashila (1); Agrawal, Yash (2); Paresh, Rutu (3); Mekita, Girish Kumar (4)	Liu, Xunde; Jin, Zhi; Tatsumi, Hiroaki; Nishikawa, Hiroshi
	Applied Materials India Pvt Ltd., India; Applied Materials, Inc.; Applied Materials, Singapore	Institute of Microelectronics, Singapore	Nanyang Technological University, Singapore; Temasek laboratories@NTU, Nanyang Technological University, Singapore	Park, DaeYoung; Jeen, Hyeongil; Kim, GiJeong; Yang, JiHeon; Sang, KwangSoo; Kim, Byungjin; Khim, JinYoung	Dhirubhai Ambani Institute of Information and Communication Technology, Gandhinagar, India; Vidya Jyoti Institute of Technology, Hyderabad, India	Osaka University, Japan
9:30am - 9:50am	**A1.4 Advanced Packaging using Chiplets and Standardized Physical Interfaces**		**A3.4 Soft-mask based Dry Etching of Parylene AF4 for Advanced Packaging Applications**	**A4.4 Development of a PCB-Embedding Technology based-79GHz MMIC Radar Frontal Module for Automotive Driving**	**A5.5 Time-domain Reflectometry Analysis on low impedance marginal failure and multi-chip modules**	**A6.4 Partial Under-fill Impact Study on Solder Joints Reliability in Smartphone Application**
	Hopsch, Fabian; Ahmed, Maudood; Heinig, Andy		Sellland, Mohamed Lamine Fayçal; Andrianov, Nikolai; Kaulfold, Robin; Miskovic, Goran	Techoban, Christian	Sasu, Leena (1); Radhamony, Rahul Babu (1); Soriano, Andrea (1); Tan, Grace (1); Yong, Sheng (2)	Pan, Ling (1); Che, Faxing (1); Ong, Yaw Chon (1); Ng, Hong Wei (1); Sinha, Kouster (2); Chen, Ting Wen (3)
	Fraunhofer IISEAS, Germany		Silicon Austria Labs GmbH, Austria	Fraunhofer IZM, Germany	Qualcomm Global Trading Pte Ltd, Singapore; Advantest (Singapore) Pte Ltd	Micron Semiconductor Asia Pte Ltd, Singapore; Micron Technology, Inc.; Micron Memory Taiwan Co
9:50am - 10:20am	Coffee/Tea Break (Waterfront Foyer)					

	Veranda I	Veranda II	Veranda III	Riverfront I	Riverfront II	Riverfront III
Session Chair	Rathin Mandal, Institute of Microelectronics	Yu-Po Wang, SPIL	Xu Kun, Applied Materials	SeokHo Na, Amkor Korea	Anandaroop Bhattacharya, IIT Kharagpur	SungSig Kang, Heraeus Materials Singapore
10:20am -11:40pm	B1: Thermo-mechanical Modeling & Simulation I	B2: Hybrid Bonding Processes and Materials 2	B3: Wafer Level Processing II	B4: Leadframe and Substrate Manufacturing II	B5: Thermal Management & Characterization I	B6: Soldered and Sintered Interconnections II
10:20am - 10:40am	**B1.1 Study on Substrate Crack through Experiment and Simulation on SSD SGA under Temperature Cycling Test**	**B2.1 Chip-to-Wafer Hybrid Bonding for high performance 2.5D applications**	**B3.1 Novel Integration Scheme to Pattern Low Cost Sub-100nm Dimensions Patterning Not Is based Sensor Devices using Self-assembled Block Copolymer (BCP) Lithography**	**B4.1 Failure Analysis of QFN Surface Discoloration by Copper Redeposition**	**B5.1 Holistic Understanding of Best Engineering Practice to Extend Cooling Limit of Next Generations of GPU**	**B6.1 Bonding with Zn-based Solders Through Self-Propagating Exothermic Reaction to Enable High-Temperature Electronics Packaging**
	Yu, Wei; Chie, FaXing; Ong, Yeow Chon; Ng, Hong Wen	Chong, Ser Choong; Cerero Daniel, Ismael; Vasarla Nagendra, Sekhar; Lim, Pei Siang; Vempati, Srinivas	Panet, Abhilash; Cummins, Cian; Sasseandran, Sandeep S; Tezcan, Deniz S	Ramiaiya Jr., Salvador Cruz (1); Rondarea, Christian Camero (2)	Haba-Ahmed, Gamal; Islam, Md Malekiul; Kabbani, Hussain; Cader, Tahir; Alissa, Hussein; Do, Hoa	Liu, Canyu (1); Jiang, Han (1); Liang, Shuitao (1); Liu, Allan (1); Zhou, Zhaoxia (2); Liu, Changqing (1)
	Micron Semiconductor Asia Operations, Singapore	Institute of Microelectronics, Singapore	Imec, Belgium	STMicroelectronics, Laguna, Philippines	AMD, United States of America; Meta; Nvidia; Microsoft	Wolfson School of Mechanical, Electrical and Manufacturing Engineering, Loughborough University; Loughborough Materials Characterisation Center, Loughborough University
10:40am - 11:00am	**B1.2 Thermo-mechanical Characterization and Stress Simulation of Epoxy Molding Compound for a High-Power SMD with Silicon Nitride Passivation Layer**	**B2.2 Fluxless Bonding Via In-Situ Oxide Reduction**	**B3.2 Optimization of Annealing Process to Realize RDL layers on High Topography Wafer for Heterogeneous Integration**	**B4.2 Board-level reliability performance comparison of Thin and Thick Ni plating ENEPIG finishes LGA and BGA packages**	**B5.2 Numerical Simulation for Flow Boiling in Microchannels with Different Pin Fin Arrays**	**B6.2 Modifying of Tin based solder composition with optimized Bi, Ni and Cu contents for high TC and drop shock reliability**
	L. Zhiwen (1); Gerete, April Joy (1); Zhou, Zhou (1); Fan, Haibo (1); Holgado, Elmer (2); Liu, Ibarra (2)	Adeel Bajwa, Tom Palumbo, Tom Coleatino, Bob Chylak, Samuel Goh	Menugu, Srinivas; Lee, Jae-wung; Singh, Navab	Tihun, SeokPhyo; Kim, JooYeop; Raj, Arun	L. Hongqing (1); Pan, Lun Sheng (1); Liu, Jing (1); Zhang, Xiaoxu (2); Lu, DuWei (1); Zheng, Ming (1); Li, Jun (1); Kang, Chang Wei (1); Chu, Xing-Jen (2); Feng, Huicheng (2)	Son, Jae Yeol (1,2); Lee, Seulgi (1); Park, Jiwon (1); Lee, Yeongseo (1); Jung, Seung-Boo (2)
	Nexperia Hong Kong; Nexperia Philippines	Kulicke & Soffa Industries Inc., Fort Washington, PA,	Institute of Microelectronics, Singapore	Analog Devices, Inc. Seoul, Korea; Analog Devices, Inc. Wilmington, MA, USA	HPC; Singapore; IME, Singapore	MICE / Sungkunkan University, Korea; Sungkyunkwan University
11:00am - 11:20am	**B1.3 A Comprehensive Study on Die Strength and Impact on Package Design**	**B2.3 Demonstration of 10nm Overlay Accuracy for Wafer-to-Wafer Bonding and Further Improvement Study**	**B3.3 Determination Behaviour Study of AF4 Parylene Thin Films on Si and SiO2 substrates by Scratch Testing**	**B4.3 Surface Stability and Surface Plasma Treatment of Different Cu Surfaces for Leadframe-to-Mold Adhesion Improvement**	**B5.3 Comprehensive Thermal Investigation of Antenna in Package for 5ATCOM On The Move**	**B6.3 Low Temperature Material for 1st Level Interconnect in Semiconductor Packaging**
	Mitsuishi, Hajime; Mori, Hiroshi; Maeda, Hidehiro; Ushijima, Mika; Aramata, Masanori; Fukuda, Hiromu; Okada, Masashi;Kanbayashi, Masahiro;Shimoda, Tomihisa;Sagaya, Isao	Simeri, Teubert; Miskovic, Goran	Fernandez, Mathew Mondala; Pulusan, Marty Lorgino Dilaunan; Estolano, Janice Marsha	Hen, Yong; Sun, Mei	Lim, Sze Pei (1); Anon, Charles (2); Sweatman, Keith (3); Tsuchya, Masahiro (4)	Lim, Sze Pei (1); Anon, Charles (2); Sweatman, Keith (3); Tsuchya, Masahiro (4)
	STMicroelectronics, Singapore	NIKON CORPORATION, Japan	Silicon Austria Labs GmbH, Austria	Amphenol Philippines Inc., Philippines	Institute of Microelectronics, A*STAR, Singapore	Indium Corporation, Malaysia; IBM Corporation; Nihon Superior Co. Ltd.; INEMI
11:20pm - 11:40pm	**B1.4 Parametric Study on Relevant Design and Material Parameters for Reliable Hard Encapsulation of Automotive Power Modules**		**B3.4 Through Silicon Via Oxide Etch Back for Via-last Integration Scheme**	**B4.4 Comparison of Mechanical Properties of Nickel-Palladium Plated and Tin-Plated Copper Leadframe Material at Elevated Temperatures**		**B6.4 Pressure Cu sintering paste for High Power devices Die attach applications**
	Sprenger, Martin (1,2); Nott, Niklas (1,2); Hecht, Christoph (2); de Greiff, Malte (1); Moller, Lukas (1); Franke, Jörg (2)		Cheemalamarri, Hemanth Kumar;Senthilkumar, Darshini;Bhawalli, Chandra Rao	Zhu, Xintong; Rajoo, Ranjan; Niaiela, Ramesh Rao; Mo, Zhi Qiang		Li, Hongyun; Ma, Li; Han, Xuelian; Yao, Min; Chen, Fen; Liu, Yan
	Vitesco Technologies Germany GmbH, Germany; Institute for Factory Automation and Production Systems (FAPS), Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany		Institute of Microelectronics, Singapore	Globalfoundries Singapore Pte Ltd		Indium Corporation, Suzhou, Jiangsu, China; Indium Corporation, 36 Robinson Road, Clinton NY

Interactive Presentations 1 at Waterfront Foyer (2:25pm to 3:55pm)

	Veranda I	Veranda II	Veranda III	Riverfront I	Riverfront II and III (Combined rooms)
Session Chair	Jeffrey C. Suhling, University of Auburn	Amr Helmy, University of Toronto	YY Tan, Yole Intelligence	Chai Tai Chong, Institute of Microelectronics	Han Yong, Institute of Microelectronics
2:25pm - 3:25pm	C1: Thermo-mechanical Modeling & Simulation II	C2: Advanced Optoelectronics and Displays	C3: Assembly Manufacturing and Tests	C4: Lithography and Laser Direct Imaging	C5: Thermal Management and Characterization II
2:25pm - 2:45pm	**C1.1 Study on Solder Joint Shape Impact on Board-Level Reliability for Managed NAND Mobile Package**	**C2.1 Laser Integration in Silicon through Flip-chip Bonding with Efficient Coupling**	**C3.1 On-the-fly Material Characterization Tool in mm-Wave and Beyond using Terahertz Time-Domain Spectroscopy**	**C4.1 Mask-less Laser Direct Imaging & Adaptive Patterning Solution for Fan-Out Heterogeneous Integration on 600mm**	**C5.1 Roadmap and Challenges on the Next Generation of Thermal Interface Material for High Wattage Heterogeneous Package**
	CHE, Fa XIng; ONG, Yeow Chon; PAN, Ling; YU, Wei; NG, Hong Wen	Chi, Ting Tai; Li, Nanxi; Cai, Hong; Li, Zhenjie; Tobing, Landobasa; Yu, Haibao; Lee, Lennon Yao Ting; Lee, Wen	Kato, Eiji (1); Kuwahara, Akira (1); Hachimoto, Masachi (1); SHANG, YANG (2)	Sasatomo, Clifford (1); Obias, Timothy (1); Fang, Jan-Kuang (2); Yang, Ping-Feng (2); San Jose, Benedict (1); Derik, Rialin (1); Huang, Sheng Feng (2); Shen, Ping-Ching (2)	Rafai-Ahmed, Gamal; Do, Hoa; islam, MD; Strader, Jason; Arellean, Quanmu; Huttunen, Jari
	Micron Semiconductor Asia Operations Pte. Ltd. Singapore	Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Singapore	ADVANTEST Corporation, Japan; ADVANTEST Singapore	Deca Technologies, United States of America; ASE Technology, Taiwan	AMD, United States of America; Laird, United States of America; Microsoft; Nokia
2:45pm - 3:05pm	**C1.2 Thermal and Warpage Analysis of High Data Rate Interconnect**	**C2.2 An EIC on PIC Packaging Solution for Photonic Engine of 800G Data Rate and Beyond**	**C3.2 Continuous Improvement on the Implementation and Computation of Statistical Yield Limits (SYL) and Statistical Bin Limits (SBL) at Final Test**	**C4.2 Lithography process optimization to realize RDL layers on high topography wafer for heterogeneous integration**	**C5.2 Design and development of manifolds for parallel flow and counter flow in two-phase cooling of 3D ICs**
	Ulaed, Mohammed; Pemidighantam, Ramana; Velurpati, Rohin Kumar; Perumaka, Shuddi Kumar	Xu, Feng; Lim, Teck Guan; Lee, Wen; Zhou, Lin	Custodio, Floralyn; Lalao, Hannaliyah; Arano, Adehl	Menugu, Srinivas; Sek, Soon Ann; Singh, Navab	Feng, Huicheng (1); Tang, Gongyue (1); Zhang, Xiaowu (1); Lau, Boon-Long (1); Jiang, Ming-Ching (1); Chui, King Jen (1); Lou, Jing (2); Li, Hongqing (2); Le, Duc Vinh (2)
	Lightspeed Photonics Private Limited., Singapore	Institute of Microelectronics, A*STAR	AMPLEON, Philippines	Institute of Microelectronics, Singapore	Institute of Microelectronics, A*STAR, Singapore; Institute of High Performance Computing, A*STAR, Singapore
3:05pm - 3:25pm	**C1.3 FEA Simulation and Modeling for Fan-Out Package Design**	**C2.3 Line Edge Roughness Optimization of Photonics Components in Electronics Photonics Heterogeneous Integration**	**C3.3 In-line Test Structures for Yield Enhancement in Microfabrication/mechanical Devices**	**C4.3 Digital Lithography for Advanced Packaging and Heterogenous Integration**	**C5.3 Reduced Order Modeling of ACET Driven Flows for Cooling of Localized Hotspots in CPUs**
	Mandal, Rathin	Sundaram, Arvind; Tew, Chin Khang; Tan, Gao Wei; Yu, Haibao; Venkataraman, Nandini; Chandra Rao, B.S.S.; Singh, Navab	Sharma, Jatin; Koh, Yul; Ghosh, Saptik; Wong, Han Xuan; Ee-Yuan Lee, Joshua	Dalacher, Bernd; Schmitzer, Sebastian; Matthias, Thorsten; Povoday, Boris; Bögelsack, Frank; Holly, Roman; Zenger, Tobias; Uhrmann, Thomas; Thallner, Bernd	Sarkar, Madhusree; Kunti, Golak; Chakraborty, Suman; Bhattacharya, Anandaroop
	Institute of Microelectronics, Singapore	Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Singapore	Institute of Microelectronics, Singapore	EV Group, Austria	Indian Institute of Technology Kharagpur, India
3:25pm - 3:55pm	Coffee/Tea Break (Waterfront Foyer)				

	Veranda I	Veranda II	Veranda III	Riverfront I	Riverfront II and III (Combined rooms)
Session Chair	John H Lau, Unimicron	Lim, Sze Pei, Indium	Ming Xue, Infineon	Ah-Young Park, KIMM	Bernd Dielacher, EV Group	Gaurav Mehta, Applied Materials
3:55pm - 5:15pm	D1: Fan-Out Packaging	D2: Assembly Materials and Processing I	D3: Quality, Reliability & Failure Analysis	D4: Samiconductor Manufacturing & Deep Learning	D5: Emerging Technologies	D6: Assembly and Manufacturing Technology I
3:55pm - 4:15pm	**D1.1 Fan-Out Higher RDL Layer Structure for Heterogeneous Solution in HPC Application**	**D2.1 Thermal Stability Characterization of High Temperature Solders in Power Surface Mount Devices**	**D3.1 Moving Limits: A More Effective Approach in Outlier Screening at Final Test**	**D4.1 Through-Focus Optical Scanning Microscopy for Embedded Defect Detection and Classification**	**D5.1 Investigation of Au-Au/In Bonding Below Eutectic Temperature for Gigahertz Bulk Acoustic Wave Transmission**	**D6.1 Ultra Thin Die pickup: Peel Stage and Pickup tool Design Comparison**
	Kao, Feng; Wang, David; Li, Sam; Shih, Terry; Chang, L.C.; Wang, Yu-Po	Le, Fred Fuliang; Guan, Zunyu; Chen, Haibin; Chae, Wing Onn; Santican, Haima	Lim, Kenneth Kristoffer; Francisco, Edgene; Abug, Gae Lenny Ruth	Lee, Jun Ho (1); Jo, Ji Yong (1); Lee, Jung Min (1); Park, Ji Won (1);Jeong, Junhee (2); Baek, Oh-Hyung (2)	Chen, Daniel Su-Han (1); Wei, Eva Leong Ching (1); Yeo, Yi Xuan (1); Sharma, Jasbir (1); Lai, Amit (2); Chai, Kevin Tshun Chuan (1)	Behler, Stefan; Pulla, Brian
	Siliconware Precision Industries Co. Ltd., Taiwan	Nexperia Hong Kong, Hong Kong S.A.R. (China); HK University of Science and Technology; Nexperia Seremban,Nexperia Philippines	Amplexon Philippines, Inc.	Kongju National Univ., Korea, Republic of (South Korea); Nextin, Korea, Republic of (South Korea)	Institute of Microelectronics, A*STAR, Singapore; SonoMEMS Laboratory, School of Electrical and Computer Engineering, Cornell University, Ithaca, NY, USA	Besi Switzerland AG, Switzerland
4:15pm - 4:35pm	**D1.2 Determination between dielectric layers of FOPLP due to copper residue under high temperature storage conditions**	**D2.2 Reversed Laser Assisted Bonding (R-LAB) Technology for Chiplet Module Bonding on Substrate**	**D3.2 Study of Moisture Penetration in Epoxy Encapsulant by Deuterium Oxide (D2O) Isotope Tracing Technique**	**D4.2 Improved Bump Detection and Defect Identification for HBMs using Refined Machine Learning Approach**	**D5.2 Fabrication of Slow Lens Miniaturized AgAgCl Reference Electrodes**	**D6.2 Understanding the Impact of Spindle Rotation Direction in the Full Cut Singulation Process of Wettable Flank QFN Packages**
	Yu, Yaoneseop (1); Ha, Job (1); Park, Mijin (1); Yang, Eunju (2); Kim, Myung (2)	Na, Seokho; Gim, Minho; Kim, Gaehyun; Ryu, DongSu; Park, DongJoo; Kim, JinYoung	Lao, Lois Jinzhi	Kwandar, Musafargani; Chen, Yu; Ming, Hua-Yuan	Gleandher, Musafargani; Chen, Yu; Ming, Hua-Yuan	Gerpott, Robin Kenneth;Listengiro, Soneda, Alvin Salloman; Antiano Jr., Ernesto Tarsian
	Samsung Electronics, Korea; Samsung Electro-Mechanics, Korea	Amkor Technology Korea, Korea, Republic of (South Korea)	AlinTech Nano-Technology Services Pte. Ltd., Singapore	Institute for Infocomm Research (I2R), A*STAR, Singapore	Institute of Microelectronics, A*STAR, Singapore	STMicroelectronics, Inc.
4:35pm - 4:55pm	**D1.3 SIC Fan-out Wafer Level Package for High Power Application**	**D2.3 Characterization of QFT Substrates at mm-wave Frequencies**	**D3.3 Board Level Life Assessment of Large Body Flip Chip Packages with Smaller Solder ball pitch & Methodologies to Improve Board-level Reliability**	**D4.3 Defect Classification using Deep Learning for Hybrid Bonding Application**	**D5.3 Multi-Sensors Characterization for Moveable Catheter Application**	**D6.3 Defining the Appropriate Reflow Profiling Set-up for Molded Air Cavity Package**
	Madowalak, Piotr (1); Wittler, Olaf (1); Braun, Tanja (1); Erbacher, Kolja (1); Conrad, Janine (1); Schiffer, Michael (1);Schneider-Ramelow, Martin (2)	Rotaru, Mihai; Bhaskar, Vignesh; Bera, Lakshmi; Singh, Navab; Han, Michael	Ramasamy, Anandan; Singh, Inderjit; Ng, Ace; Maloney, Gerry; Shao, Alan; Low, Shin Liang	Komatireddi, Rahul Reddy; Dengayach, Sachin; Rupa, Sneha;Cherikkallil, Rohith; Lewis, Prayudi	Yap, James Ven Wee; Lim, Ruiqi; Damaleto, Maria Ramona Ninfa Bautista; Cheng, Ming-Yuan	Rivera, Olga, Miranda, Jan Joseph, Tinao, Marjorie
	Fraunhofer IZM, Germany; Technische Universität Berlin, Germany	Institute of Microelectronics ASTAR, Singapore	AMD	Intel Corporation, India	Applied Materials, India	Institute of Microelectronics, A*STAR, Singapore; AMPLEON, Philippines;
4:55pm - 5:15pm	**D1.4 Process Development of Fan-Out with Multi-layer RDL for Chiplets Packaging**	**D2.4 Performance Analysis and Impact of Manufacturing Tolerances of Multi-layers Package Substrates for 5G mmWave Antenna in Package/Module (AiP/AiM)**			**D5.4 User-Interactive Light Emitting Capacitor Display For Instantaneous Liquid And Semiconductor Visualization**	**D6.4 Optimization of Process Parameters for Molding Simulation of Open Cavity QFN**
	Hsiao, Heiang Yao; Ho, Soon Wee; Lim, Pei Siang	Ho, Cheng-Yu; Huang, Hong-Sheng; Hsieh, Sheng-Chi			Qi, Xiaoying; Wu, Ruiger; Lok, Boon Keng; Fan, Wei	Lo, Shih Kuo; Jian, Ting Yu; Li, Zong Yuan; Chen, Tzu Cheh; Liu, Hui Chung; Lai, Lu Ming; Chen, Kuang Hsiung
	Institute of Microelectronics (IME), A*STAR, Singapore	Advanced Semiconductor Engineering (ASE), Inc, Taiwan			SMTech, ASTAR, Singapore	ASECL, Taiwan

DEC 9, 2022 (Friday)

	Veranda I	Veranda II	Veranda III	Riverfront I	Riverfront II	Riverfront III
Session Chair	Zhu Wenhui, Central South University	Fen Chen, Cruxes LLC	YY Tan, Yole Intelligence	Singh, Shiv Govind, IIT Hyderabad	Clifford Paul Sandstrom, Deca Technologies	Chee Ping Lee, Lam Research
08:30am - 09:00am	Invited Presentations A	Invited Presentations B	Invited Presentations C	Invited Presentations D	Invited Presentations E	Invited Presentations F
	Understanding of Hybrid Bonding Mechanism by Utilizing Molecule Simulation Approach	**Path Finding to Maximization of AI/HPC/GPC System Performance**	**Surface Activated Bonding for 3D and Heterogeneous Integration**	**Submicron Nanosecond Thermoreflectance Imaging for Thermal and Failure Analysis**	**Advanced Fan-Out Packaging for Chiplet Integration,**	**Hybrid Bonding – State-of-the-Art and Upcoming Requirements in W2W and D2W**
	Dr Minwoo Rhee, Samsung	Dr Gamal Refai-Ahmed, AMD	Prof Tadatomo Suga, University of Tokyo	Dr Mo Shakouri, Microsanj	Dr Yu-Po Wang, SPIL	Dr Bernd Dielacher, EV Group
09:00am -10:00am	E1: Thermo-mechanical Modeling & Simulation III	E2: RF Modeling, Designs and Characterizations	E3: Wire Bonding and Reliability I	E4: Solder Interconnections Reliability	E5: Wafer Level Processing III	E6: Smart Manufacturing & Equipment Tech
9:00am - 9:20am	**E1.1 PCB Design Parameters of Reducing Copper Trace Crack under Temperature Cycle Test**	**E2.1 RF Characterization and Analysis of Coplanar Waveguide on Various Silicon Wafers for 2.5D Integration**	**E3.1 Chlorine and Sulfur Effects on Copper-Aluminum Wire Bond Reliability**	**E4.1 Microstructural and mechanical integrity of CuCu joints formed through transient liquid bonding with Cu-Sn nanocomposite interlayer**	**E5.1 Reducing the Thermal Budget in Low-Temperature Polyimide Dielectric Cure for Laser Direct Image Patterning in Advanced Backend Applications**	**E6.1 Laser-Induced Forward Transfer for Assembly of Silicon Micro-Chiplets**
	Chen, Ting-Wen; Yang, Chuck; Pan, Ling; Che, Fa Xing; Ong, Yeow Chon; Sinha, Rousko; Gerusy, Christopher	Zhou, Lin; Wu, Jiaqi; Loh, Woon Leng; Jung, Ming Ching; Lim, Teck Guan	Liao, Lois Jinzhi	Jiang, Han; Robertson, Stuart; Liang, Shuibao; Zhou, Zhaoxia; Zhao, Ligun; Liu, Changqing	Karon, Zia (1); Song, Kay (1); Sandstrom, Cliff (2); Sam Jose, Benedict (2); Yamazaki, Kenta (3); Sato, Naoki (3); Yoshi, Yuki (3)	Kannoja, Harindra Kumar (1,2); Van Steenbergie, Geert (1,2)
	Micron Memory Taiwan Co; Micron Semiconductor Asia Pte Ltd, Singapore; Micron Technology, Inc., United States of America	Institute of Microelectronics, Singapore	AlinTech Nano-Technology Services Pte. Ltd., Singapore	Loughborough University, UK	Yield Engineering Systems (YES), Fremont, CA, USA; Deca Technologies, Tempe, AZ, USA ;Fujitsu Corp., Shizuoka, Japan	imec, Belgium; Ghent University, Belgium
9:20am - 9:40am	**E1.2 Package Simulation Including Effect of Process and MC Curing Shrinkage**	**E2.2 Embedding of Thinned RF Chips and Electrical RDL Characterization**	**E3.2 Detection of Bond Wire Failure in Power Semiconductors by Adjacent Temperature Sensors**	**E4.2 A Study on Combination of ENEPIG Surface Finish and Solder Ball for Solder Joint Reliability**	**E5.2 Reduction of Aluminum Fluoride Residue during Fluorinated Plasma Etching of Dielectric Passivation Layer over Aluminum Pad**	**E6.2 Improving Wire bonding Failure Classification Across Bond Recipe via Machine Learning**
	GU, BIN	Yin, Ran (1,2); Nowegbuwski, Krzysztof (1,2); Meier, Karsten (1); Bock, Karlheinz (1,2)	Jahn, Nilki; Pfeuf, Martin	Sim, Geondo; Park, Jongmin; Lim, Hunjung; Jung, GooJin	Senthilkumar, Darshini; Lim Tien Shee, Kelvin; Bhawalli, Chandra Rao	Hew, Bork Hang; Lim, Kar Wai; Suk, Yiping; Wang, Yi Bin; Song, Jenes Kang Yew
	STMicroelectronics, Singapore	Department of Electrical and Computer Engineering; Centre for Tactile Internet with Human-in-the-Loop (CeTI)	TU Dortmund University, Germany	Amkor Technology Korea, Korea, Republic of (South Korea)	Institute of Microelectronics, Singapore	ASMPT, Singapore
9:40am - 10:00am	**E1.3 Wafer Warpage Optimization Via Finite Element Analysis for a 3D Chiplet Package**	**E2.3 Role of Silicon Surface Interface and Deep Traps on the Dielectric Breakdown Performance of Epoxy Molding Compounds (EMC)**	**E3.3 High Reliability Performance of Agcored Au Coated Wire capable of Bonding to Gas Free Condition**	**E4.3 Reliability of Lead Free Solders for Die Attach in Automotive Power Modules**	**E5.3 Advanced Cu to Seed Spider Technologies for Glass Substrates with Through Glass Via and Through Glass Capacitor and Low-K Polymer Laminated Glass Substrates**	**E6.3 Finishing Degradation of Die-to-die Alignment on the Kulicke and Soffa UltraCu 500 Stepper**
	Ji Lin; Chai, Tai Chong; Lim, Sharon Pei Siang	Chua, Lin Xiao (1,2); Wee, Hui Min (2); Yong, Khai Seen (3); Li, Wu-Hsi (3); Tan, Lay Poh (1); Gan, Chee Lip (1)	Jeon, Sung min; Kim, Sang Yeob; Lee, Sung Young; Park, Hyun Jun; Ra, Mi Rang; Cho, Sung Ho; Moon, Jeong Tak	Hinojar, Bielina (1); Hachamovitch, Joshua (1); Kilang, Sebastian (1); Jerdonia, Regan (1); Luna, Sebastian (1); Sprenger, Mario (1); Mollet, Dr. Lars (1); Guth, Dr. Christian (1); Franke, Prof. Dr. Jörg (2)	Roland Kertzscheuer; Ralph Zoberbier; Patrick Carassiti; Suresh Kumar Singaravel; Stanley Izaac	Kulicke & Soffa Lilas BV, the Netherlands; CEA LETI, France
	Institute of Microelectronics Singapore, Singapore	Nanyang Technological University, Singapore; Sumitomo Bakelite Singapore Pte. Ltd; Infineon Technologies Asia Pacific Pte. Ltd	MK Electron co., Ltd, Korea, Republic of (South Korea)	Vitesco Technologies Germany GmbH, Germany; Institute for Factory Automation and Production Systems Friedrich-Alexander University Erlangen – Nürnberg	Kurtz AG	
10:00am -10:30am	Coffee/Tea Break (Waterfront Foyer)					

	Veranda I	Veranda II	Veranda III	Riverfront I	Riverfront II	Riverfront III
Session Chair	Navas Kalandar, Infineon Technologies	Min Woo Rhee, Samsung	Srinivasa Vempati, Institute of Microelectronics	Horst Theuss, Infineon Technologies	Gamal Refai-Ahmed, AMD	Bruce Kim, City University of New York
10:30am -11:50pm	F1: Assembly and Manufacturing Technology II	F2: Hybrid Bonding Processes and Materials 3	F3: Assembly Materials and Processing II	F4: MEMS and Wafer Level Processing	F5: Thermal Management & Characterization III	F6: Antenna Designs and AiP Processing
10:30am - 10:50am	**F1.1 Die Tilt Improvement Through Copper Spacers in Solder Paste Printing**	**F2.1 Process Development and Integration for Wafer-to-Wafer Hybrid Bonding**	**F3.1 Laser Package Singulation: A Promising Singulation Method for Better Package Integrity and Quality**	**F4.1 Numerical Fluidic-Chemical-Multi-Physics Simulation of a Mass Production Model for Electroless Plating of Fine-Pitch Interconnections**	**F5.1 Thermal Analysis of Power cycling Tests for a 6-in-1 Double Side Cooling SiC Power Module**	**F6.1 E-band AiP Array in 90nm CMOS FDSOI technology**
	DAN TCAN, HABIA CASIM, DCHAR, ILYAS, YAKDOU, DING, LE, FRED, LATIDO, LAUDEMER	Li, Hongmao; Chen, Gim Guan; Chui, King-Jen	Lam, Ho Hay Nicholls; Leung, Chi Ho; Chui, Chi Leung; Yeung, Shun Tik	Sophan, Bisen Jakarmas; Huang, JengHao; Shih, Po-Shan; Rengarajhan, Vengudusamy; Kung, Po-Yu; Chen, YuXn; Huang, ChingHan; Shen, ChangHsien; Kao, C. Robert	Tang, GongYue	Sun, Mei; Lim,