ADVANCE PROGRAM EPTC2023

	DAY 1: December 5, 2023 (Tuesday)						
08:00am - 08:45am	Registration						
Venue	Grand Ballroom						
08:30am - 09:00am	Opening Ceremony						
09:00am - 09:45am	**Keynote 1** Advanced System Integration Technology Trend Douglas Yu (TSMC)						
9:45am - 10:30am	**Keynote 2** Advanced Packages Enriching Heterogenous Integration Chih Pun Hung (ASE Group)						
10:30am - 11:00am	Coffee/Tea Break (Grand Ballroom Foyer)						
11:00am - 12:30pm	**Panel Session 1 - Chiplet Integration** Moderator: Zheng Jiantao (Huawei) Panelists: Ravi Mahajan (Intel), Chih Pun Hung (ASE Group), Surya Bhattacharya (A*STAR), Arvind Sundarrajan (Applied Materials)						
Venue	Grand Ballroom Foyer						
12:30pm - 1:30pm	Lunch						
Venue	Grand Ballroom						
1:30pm - 2:15pm	**Keynote 3** Will Advanced Packaging Save Moore's Law? Yang Pan (Lam Research)						
2:15pm - 3:00pm	**Keynote 4** 2.5D/3D Heterogeneous Integration for Silicon Photonics Engines Radha Nagarajan (Marvell)						
3:00pm - 3:30pm	Coffee/Tea Break (Grand Ballroom Foyer)						
3:30pm - 5:00pm	**Panel Session 2 - Artificial Intelligence for Package Design and Manufacturing** Moderator: Sam Karikalan (Broadcom) Panellists: Samuel Goh (K&S), Grace O'Malley (iNEMI), Vincent Dicaprio (Applied Materials), K.N. Chiang (National Tsing Hua University)						
6:00pm - 8:00pm	VIP Dinner (by invitation only)						
	DAY 2: December 6, 2023 (Wednesday)						
08:00am - 09:00am	Registration						
Venue	Canary 1 / Canary 2		Oriole	Pelican	Kingfisher	Nightingale	
09:00am - 10:15am	**PDC1** Fan-Out, Chiplet, and Heterogenous Integration Packaging (John H Lau)		**PDC2** Flip Chip Interconnect (Eric Perfecto)	**PDC3** Co-Packaged Si Photonics: Opportunities and Challenges (Amr S. Helmy)	**PDC4** Design-on-Simulation Technology for Advanced Packaging Reliability Life Prediction (K.N. Chiang)	**PDC5** Automotive Electronics Reliability - Challenges and Opportunities (Pradeep Lall)	
10:15am - 10:35am	Coffee/Tea Break						
10:35am - 12:00pm	PDC1 (cont'd)		PDC2 (cont'd)	PDC3 (cont'd)	PDC4 (cont'd)	PDC5 (cont'd)	
Venue	Grand Ballroom						
12:00pm - 1:30pm	EPS Luncheon EPS Presentations; Student Travel Grant Awards Ceremony; Organizing Committee Recognition						
1:30pm - 2:15pm	**Technology Talk** Challenges in the Analysis and Testing of Advanced Packaging Systems Mo Shakouri (Microsanj LLC)						
Venue	Canary 1 / Canary 2						
2:20pm-3:50pm	**Exhibitors' Presentations**						
3:50pm - 4:10pm	Coffee/Tea Break (Grand Ballroom Foyer)						
Venue	Canary 1	Canary 2	Oriole	Pelican	Kingfisher	Nightingale	
4:10pm-5:30pm	Antenna in Package	Hybrid Bonding I	Solder Materials and Processes	Mechanical Simulation & Characterization I	Smart Manufacturing and Equipment Technology	TSV and Metallization	
Session Chair							
4:10pm - 4:30pm	**A1.1 (P168) Antenna-in-Package Electrical Research for Beyond 5G application** Lai, Chia-Chu; Lin, Sam; Shih, Teny; Kang, Andrew; Wang, Yu-Po Siliconware Precision Industries Co., Ltd, Taiwan	**A2.1 (P118) High-density and high-throughput bonding technology for 3D integration** Mao, Xingchao; Chen, Yulong; TU, King-Ning; Liu, Yingxia City University of HONGKONG, Hong Kong S.A.R. (China)	**A3.1 (P155) The trend for low temperature solder (LTS) assembly** Nishimura, Takatoshi; Akaiwa, Tetsuya; Sweatman, Keith Nihon Superior Co., Ltd., Japan	**A4.1 (P105) The Phenomenon of Tunnel Structure Mold Flowability Experiment Result and Simulation Study** Lo, Shih Kun; Su, Yi Hsun; Li, Zong Yuan; Chien, Tzu Chieh; Liu, Hui Chung; Lai, Lu Ming; Chen, Kuang Hsiung ASECL, Taiwan	**A5.1 (P239) Post bonding Defect Analysis using Deep Learning** Komatireddi, Rahul Reddy; Dangayach, Sachin; Cherikkallil, Rohith; Lianto, Prayudi Applied Materials, India	**A6.1 (P265) Wafer level fabrication of Embedded Silicon Microchannel on Heating Devices** Lau, Boon Long; Ong, Javier; Au, Jason; Jong, Ming Chinq; Zhang, Xiaowu; Feng, Huicheng IME Astar, Singapore	Interactive Presentations 1
4:30pm - 4:50pm	**A1.2 (P166) Characterization of FOWLP Antenna in Packages** Sun, Mei; Lim, Teck Guan; Zhou, Lin Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Singapore	**A2.2 (P180) Finite element simulation of Cu-SiO2 direct hybrid bonding: impact of via on bonding integration** Zhao, Guoqiang (1,2,3); Wang, Wenzhi (3); Zhang, Huimin (4); Zhang, Nan (4); Zhou, Xiaofeng (4); Zhao, Yi (1,2,4) 1: College of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China; 2: International Joint Innovation Center, Zhejiang University, Haining 314400, China; 3: China Nanhu Academy of Electronics and Information Technology, Jiaxing 314001, China; 4: School of Integrated Circuits, East China Normal University, Shanghai 200241, China	**A3.2 (P263) FCPBGA C4 Abnormal Leadfree Solder Bump Prevention** Koey Poh Meng, Dominic; Ha, Khai Soon; Md Fadzil, Muhammad Fadzlan NXP Semiconductors, Malaysia	**A4.2 (P109) Numerical and Experimental Investigation of Package Warpage of Large Mold-First FOWLP** Zhang, Xiaowu (1); Lim, Sharon P. S. (1); Lau, Boon Long (1); Han, Yong (1); Jong, Ming Chinq (1); Wang, Xiaobai (2); Liu, Songlin (2) 1: Institute of Microelectronics, A*STAR, Singapore; 2: Institute of Materials Research and Engineering, A*STAR, Singapore	**A5.2 (P319) Efficient and Adaptive Semantic Segmentation of HBMs using Incremental Learning** Chang, Richard (1); Wang, Jie (1); Thakur, Namrata (1); Li, Yurui (1); Chong, Ser Choon (2); Pahwa, Ramanpreet Singh (1) 1: Institute for Infocomm Research (I2R), A*STAR; 2: Institute of Microelectronics (IME), A*STAR	**A6.2 (P358) Defect evolution during through-silicon via copper electroplating and methods for robust void-free filling** Tran, Van Nhat Anh; Venkataraman, Nandini; Tao, Meng; Tseng, Ya-Ching; Wang, Xiangyu; Chui, K.-J; Singh, Navab; Srinivasa Rao, Vempati Agency for Science, Technology, and Research - Institute of Microelectronics, Singapore	
4:50pm - 5:10pm	**A1.3 (P294) E-Band LTCC Phased Array AiP for Automotive Applications** Abdellatif, Ahmed Shehata (1); Zhai, Wenyao (1); Pothula, Hari Krishna (1); Wessel, David (1); Wang, Guangjian (2); Huang, Guolong (2); Shuai, Songlin (2) 1: Huawei Technologies, Canada; 2: Huawei Technologies, Chengdu Base	**A2.3 (P227) Grain boundary analysis of Cu-Cu hybrid bonding using ACOM-TEM** Fujimoto, Ryosuke; Yasuda, Mitsunobu; Tarumi, Nobuaki; Shinozaki, Yuko; Kawasaki, Naohiko; Otsuka, Yuji Toray Research Center, Inc., Japan	**A3.3 (P328) Modifying of solder composition as MXT03 for high TC reliability on Cu-OSP** Son, Jae Yeol (1,2); Lee, S.G (1); Lee, Y.W (1); Jung, S.B (2) 1: MKE,Korea, Republic of (South Korea); 2: Sungkunkan university, Korea, Republic of (South Korea)	**A4.3 (P258) Identify critical packaging parameters impacting wafer warpage using FEA and statistical analysis** Ji, Lin; Ng, Ng Yong Chyn Institute of Microelectronics Singapore, Singapore	**A5.3 (P364) Study on Enhancing Flip-Chip Chip Scale Package (FCCSP) Reliability Testing using Deep Learning Assisted SAM** Sukumaran Nair, Arya (1); Djuric-Rissner, Tatjana (1); hoffrogge, Peter (1); Koch, Matthias (1); Birki, Bugra (1); Ramos, Zyzi (1); Wang, Rachel (1); Czurratis, Peter (1); Ho, Hsien-Wei (2); Kuo, Chun-Liang (2); Ko, Chun-Yu (2); Yen, Justor (3) 1: PVA TePla Analytical Systems GmbH, Germany; 2: Advanced Semiconductor Engineering (ASE) Inc. Taiwan; 3: Challentech International Corp, Taiwan	**A6.3 (P348) Evaluation of C2W hybrid bonding performance with SiO2/SiCN passivate layers at interface using finite element sim** Tippabhotla, Sasi Kumar; Lin, Ji; Chong, Ser Choong Institute of Microelectronics, A*Star Research Entities, Singapore, Singapore	
5:10pm - 5:30pm	**A1.4 (P178) Design of 1THz band 4array on-chip one-sided directional antenna** Kim, Ryeong; Ryo, Takigawa; Kanya, Haruichi Kyushu University, Japan	**A2.4 (P232) RC delay mitigation for sub 700nm hybrid bonding pitch** Lhostis, Sandrine (1); Ayoub, Bassel (1,2); Fremont, Helene (2); Moreau, Stephane (3); Mermoz, Sebastien (1); Deloffre, Emilie (1); Souchier, Emeline (1); Gusmão Cacho, Maria Gabriela (1); Aybeke, Ece (1); Lamontagne, Patrick (1); Rey, Christelle (1); Tournier, Arnaud (1) 1: STMicroelectronics, 850 rue Jean Monnet, F-38926 Crolles Cedex, France; 2: IMS Laboratory, University of Bordeaux, UMR 5218, 33405 Talence, France; 3: Univ. Grenoble Alpes, CEA, LETI, 38000 Grenoble, France	**A3.4 (P347) Indium-based Flip-chip Interconnect for Cryogenic Packaging** Jaafar, Norhanani; Hongyu, Li; Ser Choong, Chong; King-Jien, Chui Institute Of Microelectronic, Singapore	**A4.4 (P137) Impact of Wafer Pre-thin Thickness on Stealth Dicing Performance** Lim, Dao Kun (1); Vempaty, Venkata Rama Satya Pradeep (2); Sim, Wen How (1); Singh, Harjashan Veer (3) 1: Micron Semiconductor Asia Operations Pte. Ltd., Singapore; 2: Micron Technology Inc., India; 3: Micron Memory Taiwan Co. Ltd., Taiwan	**A5.4 (P369) Anomaly Detection for Dispensing of Solder Paste on 3D Circuit Carriers Using Machine Learning** Thielen, Nils; Wagner, Marco; Meier, Sven; Voigt, Christian; Franke, Jörg Friedrich-Alexander-Universität Erlangen-Nürnberg, Institute for Factory Automation and Production Systems, Germany	**A6.4 (P207) Effect of PECVD thickness on warpage behavior of 3DS TSV wafer** Wang, Biao; Fan, Zengyan; Quan, Changhao; Ahn, Charles ChangXin Memory Technologies, Inc.,	
06:00pm - 09:00pm	Banquet Dinner						
	DAY 3: December 7, 2023 (Thursday)						
Venue	Canary 1	Canary 2	Oriole	Pelican	Kingfisher	Nightingale	
08:30am -09:00am	**Invited Talk 1** 3D Integrated Package for High Performance Computing Application (Yu-Po Wang, SPIL)	**Invited Talk 2** Wafer-to-Wafer and Die-to-Wafer Hybrid Bonding for Advanced Interconnects (V. Dragoi EVG)	**Invited Talk 3** Development of Novel Polymer Materials for Advanced Packaging (Takenori Fujiwara, Toray)	**Invited Talk 4** The Era of Generative AI and Advanced Packaging (Chak Wing Kei, ASMPT)	**Invited Talk 5** AI and Failure-Mechanics-Based Life Prediction for Electronic Systems (Pradeep Lall, Auburn Univ.)	**Invited Talk 6** Forward-Looking Roadmap View to Enable Heterogeneous Integration in the Next 10 Years (Gamal Refai-Ahmen, AMD)	
09:00am -10:00am	Interconnects in Advanced Packaging	Hybrid Bonding II	Materials and Processing I	Mechanical Simulation & Characterization II	Solder Reliability	Cooling Solutions for SiC	
09:00am - 09:20am	**B1.1 (P153) Challenges of Scaling Down High Power Performance Flip Chip Ball Grid Array (FCBGA) Package** Chan, Weng Hoong; Lakhera, Nishant; Uehling, Trent; Bharatham, Logendran; Shantharam, Sandeep; Mohd Sukemi, Azham NXP Semiconductor, Malaysia	**B2.1 (P237) Study of Cu Pad Expansion with Surrounded Dielectrics for Hybrid Bonding** Cheemalamarri, Hemanth Kumar; Ji, Lin; Lee, Wen; Vempati, Srinivasa Rao; Singh, Navab Agency for Science and Technology Research (ASTAR) Singapore., Singapore	**B3.1 (P103) Development of micron-sized Ag Si composite paste die attach material** Chen, Chuantong (1); Liu, Yang (1); Li, Wangyun (1); Ueshima, Minoru (2); Nakayama, Koji (1); Suganuma, Katsuaki (1) 1: Osaka university, Japan; 2: Daicel Corporation	**B4.1 (P261) Mechanical Modelling and Analysis of CMOS Image Sensor Package** Lim, Teck Siang (1); Sukiman, Muhamad Shafiq (1); Nur Diana, Izzani Masdzarif (2); Solehah, Jasmee (2) 1: ON Semiconductor (M) Sdn Bhd; 2: Universiti Teknikal Malaysia Melaka . UTeM	**B5.1 (P156) Package Design Characterization Influencing Substrate Metal Crack in BGA Package** Lim, Jasmine (1); Tran, Tu-Anh (2); Shantaram, Sandeep (2); Koh, WenShi (1) 1: NXP Semiconductors, Malaysia; 2: NXP Semiconductors, Austin, Texas	**B6.1 (P341) Transient thermal characterization and analysis for next generation SiC power module** Tang, Gong Yue; Ye, Yong Liang; Wai, Leong Ching; Han, Yong Institute of Microelectronics, Singapore	
09:20am - 09:40am	**B1.2 (P259) Thermo-Mechanical performance of large body and small ball pitch Flip chip packages using higher layer count substrates with ENEPIG solder pad finish** Ramasamy, Anandan (1); Singh, Inderjit (2); Ng, Ace (3); Maloney, Gerry (4); Low, Shin (5); Shao, Alan (6) 1: AMD, Singapore; 2: AMD, San Jose; 3: AMD, Singapore; 4: AMD, San Jose; 5: AMD, San Jose; 6: AMD, San Jose	**B2.2 (P286) LAB (Laser Assisted Bond) bonding mechanism** Kim, Gahyeon Amkor Technology Korea, Korea, Republic of (South Korea)	**B3.2 (P339) Feasibility and Optimisation of Cu Sintering under Nitrogen Atmosphere** Meyer, Jörg; Gierth, Karl Felix Wendelin; Meier, Karsten; Bock, Karlheinz Technische Universität Dresden, Institute of Electronic Packaging Technology, Germany	**B4.2 (P222) Characterization of Differential TMV Vertical Interconnects to 50GHz with Double Side Measurement** Wu, Jiaqi (1); Lim, Teck Guan (1); Liow, Jason Tsung-Yang (2); Gourikutty, Sajay Bhuvanendran Nair (1) 1: Institute of Microelectronics, A*STAR, Singapore; 2: Rain Tree Photonics Pte Ltd, Singapore	**B5.2 (P190) Reliability prediction and improvement of board-level thermal cycling test for molded FC BGA array** Chen, Dao-Long (1); Chen, Tang-Yuan (1); Lai, Wei-Hong (1); Yin, Wei-Jie (1); Kuo, Chun-Liang (2); Ko, Chun-Yu (2); Cheng, Chi-Min (2) 1: Product Characterization, Advanced Semiconductor Engineering, Inc., Taiwan; 2: Quality Assurance Laboratory, Advanced Semiconductor Engineering, Inc., Taiwan	**B6.2 (P162) Double-side Liquid Cooling Development for 6-in-1 SiC Power Module** Han, Yong; Tang, Gongyue Institute of Microelectronics, A*STAR, Singapore	
09:40am - 10:00am	**B1.3 (P264) Back Side Metalization for Logic Application** Rettenmeier, Roland (1); Zoberbier, Ralph (1); Low, Stanley (2); Singaram, Suresh Kumar (3) 1: Evatec AG, Switzerland; 2: Evatec AG, Taiwan Branch; 3: Evatec SEA Pte Ltd	**B2.3 (P303) A New Evaluation Method of Bonding Strength using Atomic Force Microscopy** Shin, Donggap; Moon, Bumki; Lee, Yongjin; Woo, Siwoong; Lee, Byungjoon; Rhee, Minwoo Samsung Electronics	**B3.3 (P179) Chemical Deburring as Process Solution for Eliminating Sn Metal Burrs of Wettable Flank QFN Devices** Serapio, Rohn Kenneth Listangco; Antilano, Ernesto Jr. Tarosan; Gablan, Alyssa Grace Sarmiento; Soreda, Alvin Salloman; Diwata, Jerry Tabilog; Niem, Cherry Joy Macasilang STMicroelectronics, Inc., Philippines	**B4.3 (P345) Mission Profile related Design for Reliability for Power Electronics based on Finite Element Simulation** Albrecht, Jan (1,2); Horn, Tobias (1); Habenicht, Soenke (3); Rzepka, Sven (1,2) 1: Fraunhofer ENAS, Technologie-Campus 3, 09126 Chemnitz, Germany; 2: Technical University Chemnitz, Center for Microtechnologies, Reichenhainer Straße 70, 09126 Chemnitz, Germany; 3: Nexperia, Stresemannallee 101, 22529, Hamburg, Germany	**B5.3 (P360) Insights into the Solder Non-wetting Failure due to Flux Inactivation and Degradation** Arellano, Ian Harvey; Sia, Jonalyn STMicroelectronics, Inc., Philippines	**B6.3 (P322) Excellent Reliability Organic Thermal Interface Materials for SiC Power Module** Fujiwara, Takenori (1); Sakabe, Yohei (2); Shimada, Akira (2) 1: Toray Singapore Research Center; 2: Toray Industries, Inc.	
10:00am - 10:30am	Coffee/Tea Break (Grand Ballroom Foyer)						
Venue	Canary 1	Canary 2	Oriole	Pelican	Kingfisher	Nightingale	
10:30am -11:50am	Hybrid Bonding in Advanced Packaging	Wirebonding Processes	Bonding Materials and Processes	Mechanical Simulation & Characterization III	Reliability I	Thermal Management I	
10:30am - 10:50am	**C1.1 (P139) Edge Detection Algorithm for Blurred Alignment Marks in Hybrid Bonding** Sugiura, Takamasa (1); Nagatomo, Daisuke (1); Kajinami, Masato (1); Ueyama, Shinji (1); Tokumiya, Takahiro (1); Oh, Seungyeol (2); Ahn, Sungmin (2); Choi, Euisun (2); Woo, Siwoong (2); Lee, Hyunjin (2); Lee, Byungjoon (2); Rhee, Minwoo Daniel (2) 1: Samsung Japan Corporation, Samsung Device Solutions R&D Japan; 2: Samsung Electronics Co., Ltd, Mechatronics Research	**C2.1 (P124) Characteristics and Reliability of Al and Al-coated Cu Wires for High Power Applications** Flauta, Randolph Estal (1); Funke, Hans-Juegen (2); Birkoben, Tom (2); Habenicht, Soenke (2); Liguda, Christian (2); Tai, King Man (1); Fan, Haibo (1); Yao, Peilun (4); Chen, Haibin (3) 1: Nexperia Hong Kong, Hong Kong S.A.R.; 2: Nexperia Germany GmbH; 3: The Hong Kong University of Science and Technology, Hong Kong S.A.R.; 4: Hong Kong University of Science and Technology (Guangzhou), Guangzhou, P.R. China	**C3.1 (P289) Exploring Bond Strength for Advanced Chiplet with Hybrid Bonding** Fuse, Junya; Iwata, Tomoya; Yoshihara, Yuki; Sano, Marie; Inoue, Fumihiro Yokohama national university, Japan	**C4.1 (P125) Design Optimization to Boost Solder Joint Reliability Performance for SSD BGA Package** pan, ling (1); che, Fa Xing (1); yu, wei (1); ong, yeow chon (1); ng, hong wan (1); Tan, Kelvin Aik Boo (1); lum, Wen wei (1); Sinha, Koustav (2); chen, ting wen (3) 1: Micron Semiconductor Asia Operations Pte. Ltd; 2: Micron Technology, Inc.; 3: Micron Memory Taiwan Co	**C5.1 (P385) Improving Board Level Reliability of Ultra Thin PCBA by Systematic Novel Solutions** Jiang, Yiming; Shi, Hongbin; Li, Mengyuan Huawei Technologies Co., Ltd., China, People's Republic of	**C6.1 (P368) Thermohydraulic Characteristics of a MEMS Heat Sinks: Zig-Zag Microchannels with Sidewall Ribs** Alnaimat, Fadi (1,2); Alnuaimi, Saeed (1,2); Mathew, Bobby (1,2) 1: United Arab Emirates University, Mech. Engineering Department, United Arab Emirates; 2: United Arab Emirates University, National Water and Energy Center, United Arab Emirates	
10:50am - 11:10am	**C1.2 (P144) Alignment Vision System for Hybrid Bonding in Advanced Packaging** Nagatomo, Daisuke (1); Sugiura, Takamasa (1); Kajinami, Masato (1); Ueyama, Shinji (1); Tokumiya, Takahiro (1); Oh, Seungyeol (2); Ahn, Sungmin (2); Choi, Euisun (2); Woo, Siwoong (2); Lee, Hyunjin (2); Lee, Byungjoon (2); Rhee Daniel, Minwoo (2) 1: Samsung Japan Corporation, Samsung Device Solutions R&D Japan; 2: Samsung Electronics Co., Ltd., Mechatronics Research	**C2.2 (P135) Copper Alloy Wire Selection Methodology for High Reliability Automotive IC packages** Fundan, Raquel Lacuesta; Renard, Loic; Orr, Geok Koon; Loo, Shei Meng STMicroelectronics Pte. Ltd., Singapore	**C3.2 (P313) Plasma Modelling Framework on Dielectric Surfaces in Hybrid Bonding Technology** Dag, Sefa (1); Jiang, Liu (1); Hung, Raymond (2); Lianto, Prayudi (2); An, Jinho (2); See, Gilbert (2); Ayyagari-Sangamalli, Buvna (1); Bazizi, El Mehdi (1) 1: Applied Materials, United States of America; 2: Applied Materials, Singapore	**C4.2 (P132) Investigation on Underfill Properties Effect on Board Level Solder Joint Reliability for SiP Package** Che, Faxing (1); Ong, Yeow Chon (1); Pan, Ling (1); Yu, wei (1); Ng, Hong wan (1); Chen, Wren (2) 1: Micron Semiconductor Asia Operations Pte. Ltd, Singapore; 2: Micron Memory Taiwan Co	**C5.2 (P146) Effects of temperature and electrical bias on Cu-Al IMCs growth** Liao, Lois Jinzhi WinTech Nano-Technology Services Pte. Ltd., Singapore	**C6.2 (P116) Experimental investigations on the chip thermal coupling effect by embedded manifold cooling** Ye, Yuxin; Kong, Yanmei; Du, Xiangbin; Liu, Ruiwen; yun, Shichang; Jia, shiqi; Jiao, Binbin The Institute of Microelectronics of the Chinese Academy of Sciences, China, People's Republic of	
11:10am - 11:30am	**C1.3 (P355) eliability Assessment of 2.5D Module using Chip to Wafer Hybrid Bonding** Chong, Ser Choong; Jason Au, Keng Yuen; Vasarla Nagendra, Sekhar; Ismael, Cereno Daniel; Mishra, Dileep; Vempati, Srinivasa Rao Institute of Microelectronics, Singapore	**C2.3 (P236) Insulated, Passivated & Adhesively-Promoted Bond Wire using Al2O3 Coating** Park, Soojae OxWires Co., Ltd., Korea, Republic of (South Korea)	**C3.3 (P354) Polymer Dielectric Materials Evaluation for Hybrid Bonding Applications** Vasarla, Nagendra Sekhar (1); Takenori, Fujiwara (2); Hitoshi, Araki (2); Yu, Shoji (2); Masaya, Jukei (2); Kota, Nomura (2); Mishra, Dileep Kumar (1); Chong, Ser Choong (1); Vempati, Srinivasa Rao (1) 1: Institute of Microelectronics, A*STAR, Singapore; 2: Toray Industries, Inc. Japan	**C4.3 (P140) Copper/Molding Compound Interfacial Delamination** Rovitto, Marco (1); Zalaffi, Samuele (1); Passagrilli, Carlo (1); Andena, Luca (2); Mariani, Stefano (2) 1: STMicroelectronics, Italy; 2: Politecnico di Milano, Italy	**C5.3 (P149) Integration of Artificial Neural Network and Finite Element Simulation for Package Warpage Prediction** Panigrahy, Sunil Kumar (1); Che, Fa Xing (2); Ong, Yeow Chon (2); Nune, Prasad Nagavenkata (1); Ng, Hong Wan (2) 1: Micron Technology Operations India LLP, India; 2: Micron Semiconductor Asia Operations Pte. Ltd. 990, Bendemeer Road, Singapore	**C6.3 (P148) High Thermal Solution for 3D Integration Package** Chen, Ching Chia; Kao, Nicholas; Lin, Shane; Li, Yung Ta Siliconware Precision Industries Co., Ltd., Taiwan	
11:30am - 11:50am	**C1.4 (P316) Optimization of CMP process for direct wafer to wafer oxide bonding** Ji, Hongmiao; Cheemalamarri, Hemanth Kumar; CHI, Ting-Ta; LIM, Hui-ting; TEO, Wei-Jie; NEO, Siang-Kiat; LI, Hong-Yu; CHEN, Gim-Guan; Venkataraman, Nandini; LEE, Wen Institute of Microelectronics (IME), A*STAR, Singapore	**C2.4 (P350) Moisture- and Saline-induced Degradation of Silver Wire and Silver|Aluminum Bond Integrity** Arellano, Ian Harvey; Sia, Jonalyn STMicroelectronics, Inc., Philippines	**C3.4 (P333) High-speed Optical Detection of Chipping Defects in a Die Bonder** Ackerl, Norbert; Wiedmer, Andreas; Zeng, Guodong; Forooghifar, Farnaz Besi Switzerland AG, Hinterbergstrasse 32a, 6312 Steinhausen, Switzerland	**C4.4 (P142) Effect of Underfill on Substrate Trace Crack under PTC** Yu, Wei (1); Pan, Ling (1); Tan, Kelvin (1); Che, Fa Xing (1); Ong, Yeow Chon (1); Ng, Hong Wan (1); Fan, Richard (2) 1: Micron Semiconductor Asia Operations, Singapore; 2: Micron Memory Taiwan Co., Ltd, Taichung city, Taiwan	**C5.4 (P172) Capacitive-based wire bonding defects detection method for integrated circuit package in strip form** Qiu, Tie (1); Khoo, Leslie (2); Tan, Joseph (1); Loo, Amy (1) 1: Keysight Technologies Singapore, Singapore; 2: STMicroelectonics	**C6.4 (P235) Impact of High Temperature Storage for Prolonged Duration on Cu Leadframe Material Properties for Automotive Applications** Zhu, Xintong; Rajoo, Ranjan; Yip, Kim Hong; Ang, Poh Chuan; Nistala, Ramesh Rao; Mo, Zhi Qiang Globalfoundries, Singapore	
Venue	Grand Ballroom						
12:00pm -1:30pm	EPTC Luncheon EPTC Highlights; Sponsorship/ Exhibition Appreciation Ceremony						
Venue	Canary 1	Canary 2	Oriole	Pelican	Kingfisher	Nightingale	
1:30pm-3:00pm	**Exhibitors' Presentations**			**Region 10 Chapter Chairs' Meeting**			
Venue	Canary 1	Canary 2	Oriole	Pelican	Kingfisher	Nightingale	
3:00pm -4:00pm	2.5D/3D Packaging Technologies	Bumping Technologies I	Materials and Processing II	Mechanical Simulation & Characterization IV	Emerging Technologies	Advanced Optoelectronics and Displays I	
3:00pm - 3:20pm	**D1.1 (P309) Packaging strategies for Photonic and Electronic chips on a Glass substrate** Bernson, Robert (1); Wakeel, Saif (1); Gupta, Parnika (1); Ranno, Luigi (2); Weninger, Drew (2); Agarwal, Anuradha (2); Serna, Samuel (3); Hu, Juejun (2); Gradkowski, Kamil (1); Kimerling, Lionel (2); O' Brien, Peter (1) 1: Tyndall National Institute, University College Cork, Ireland; 2: Massachusetts Institute of Technology, Cambridge, MA, USA; 3: Bridgewater State University, Bridgewater, MA, USA	**D2.1 (P106) low-temperature solder for low-carbon emitting process** Wang, Yi-Wun; Liang, Hua-Tui; Tseng, Tzu-Ting; Wu, Guo-Wei Tamkang University, Taiwan	**D3.1 (P182) Recycle Tin Lead-Free Solder Paste for Advanced Packaging** Audrey Long, Wee Seng; Pang, HuiShyan; Lo, Yee Ting; Jason Lim, Chze Min; Tan, Tze Qing; Kang, Sung Sig Heraeus Materials Singapore Pte. Ltd.,, Singapore	**D4.1 (P196) Hard bond pad plastic deformation study for adhesion estimation by 3D FEM modelling of wire bonding process** guarino, lucrezia; caglio, carolina; villa, riccardo; carasi, beatrice; passagrilli, carlo; cecchetto, luca STMicroelectronics, Italy	**D5.1 (P158) Flexible ICs Developed by Transferring FDSOI CMOS FETs on Plastic Substrate for CMOS Image Sensors** Goto, Masahide; Imura, Shigeyuki; Sato, Hiroto NHK Science & Technology Research Laboratories, Japan	**D6.1 (P128) Solutions for Process Challenges on Fan-Out Wafer Level Packaging of Electronic-Photonic Integration** Chia, Lai Yee; Bhuvanendran Nair Gourikutty, Sajay; Ho, Soon Wee Institute of Microelectronics, A*STAR, Singapore	
3:20pm - 3:40pm	**D1.2 (P325) Bridge Die Compensation & Adaptive Patterning in a Multi-Die Module in 600 mm Format** Sandstrom, Clifford (1); Talain, Erick (1); San Jose, Benedict (1); Fang, Jen-Kuang (2); Yang, Ping-Feng (2); Huang, Sheng-Feng (2); Shen, Ping-Ching (2) 1: Deca Technologies, United States of America; 2: ASE Technology, Taiwan	**D2.2 (P371) Investigation of SnAg Superconductivity as Solder Material for Cryogenic Packaging** Ng, Yong Chyn (1); Li, Hongyu (1); Binte Jaafar, Norhanani (1); Goh, Kuan Eng Johnson (2,3,4); Huang, Ding (2); Lau, Chit Siong (2); Lee, Rainer Cheow Siong (2); Chui, King-Jien (1) 1: Institute of Microelectronics (IME), Agency for Science Technology and Research (A*STAR); 2: Institute of Materials Research and Engineering (IMRE), Agency for Science Technology and Research (A*STAR); 3: Department of Physics, National University of Singapore (NUS); 4: Division of Physics and Applied Physics, School of Physical and Mathematical Sciences, Nanyang Technological University (NTU)	**D3.2 (P197) A Novel Approach to Enhance the High-Reliability of Solder Joints through Pneumatic Reflow Technology** Su, Huan Ping; Hsu, Ming Hua; Chen, Chih Hsiung; Horng, Auger Ableprint Technology Co. Ltd., Taiwan	**D4.2 (P329) Study on Using Noisy Synthetic Data for Neural Networks to Assess Thermo-Mechanical Reliability Parameters of Solder Interconnects** Albrecht, Oliver; Höhne, Robert D. J.; Barkur, Dharshan; Meier, Karsten; Bock, Karlheinz Technische Universität Dresden, Institute of Electronic Packaging Technology, Dresden, Germany	**D5.2 (P351) Process Development and Integration on Si Substrate for Ion trap-based Quantum Processors** Li, Hongyu (1); Liu, Clarence Liu Huihong (2); Jaafar, Norhanani Jaafar (1); Ahmadi, Morteza Ahmadi (2); Mishra, Dileep (1); Chun, Goh Chun Kiat Simon (1); Zhou, YanYan (1); Mukherjee, Manas (2,3); Chui, King Jien (1) 1: IME, Singapore; 2: CQT/NUS, Singaproe; 3: IMRE, Singapore	**D6.2 (P133) Design and Fabrication of a Test Board assembly for a Silicon Photonics LiDAR Device** Shaw, Mark (1); Fincato, Antonio (1); Maggi, Luca (1); Caltabiano, Daniele (1); Carastro, Filippo (1); Rotta, Davide (2); Serrano Rodrigo, Aina (2); Chiesa, Marco (2); Bajoni, Daniele (3); Galli, Matteo (3); Gianini, Linda (3,4); Diotti, Paolo (1) 1: STMicroelectronics Srl, Italy; 2: Camgraphic Srl; 3: University of Pavia; 4: Univ. Grenoble Alpes, CEA-LETI, 38054 Grenoble, France	
3:40pm - 4:00pm	**D1.3 (P331) BoW Die to Die interface implementation: An open standardized interface for future Electronics** Ahmed, Maudood; Heinig, Andy; Kadam, Sneha; Navilipuri, LavaKumar Fraunhofer Institute for Integrated Circuits IIS Division Engineering of Adaptive Systems EAS, Germany	**D2.3 (P126) Effect of Reflow on Solder Joint in Low Temperature SnBi Solder Paste** Balasubramanian, Senthil Kumar; Chiong, Kenny; Sutiono, Sylvia; Sarangapani, Murali; Lo, Miewwan; Zhang, HanWen; SungSig, Kang Heraeus Materials Singapore Pte Ltd, Singapore	**D3.3 (P204) High Thermal EMC Solution Applied in Thin FCCSP** Su, Pin-Jing; Hung, Liang-Yih; Chen, Carl; Wang, Yu-Po SPIL, Taiwan	**D4.3 (P247) Strain rate effect of nickel-based single crystal superalloy revealed by nanoindentation** Shen, Ziyi; Su, Yutai; Long, Xu Northwestern Polytechnical University, Xi'an, People's Republic of China	**D5.3 (P372) Vertical Hexagonal Arrangement Structure - VHAS** Sahoo, Akanksha Micron, India	**D6.3 (P315) A novel packaging solution for 400G photonic engine** xu, feng; li, zhenyu; Lee, wen A*STAR, Singapore	

4:00pm - 4:20pm	Coffee/Tea Break (Grand Ballroom Foyer)						Interactive Presentations 2
4:20pm-5:40pm	Advanced Packaging Technologies I	Hybrid Bonding III	Processes for Emerging Devices	Mechanical Simulation & Characterization V	Failure Analysis I	Advanced Optoelectronics and Displays II	
4:20pm - 4:40pm	**E1.1 (P157) 2-D MODELLING OF FAN-OUT PANEL LEVEL PACKAGE AND ITS WARPAGE SUPPRESSION SOLUTION** Singh, Shivendra Pratap; Pancham, Padmanabh Pundrikaksha; Lo, Cheng-Yao National Tsing Hua University, Taiwan	**E2.1 (P318) Polymer Based Dual Damascene Process for Fine Pitch RDL Advanced Packaging** Hsiao, Hsiang Yao (1); Ley, Ryan (2); Suo, Peng (2); Yong, Andy Chang Bum (2) 1: Institute of Microelectronics / Agency for Science, Technology and Research, Singapore; 2: Packaging Process Integration, Applied Packaging Development Center, Applied Materials, Inc.	**E3.1 (P213) Patterned Fabry-Perot Filter Fabrication on Transparent wafer in 200mm CMOS fab** Yoo, Tae Jin; Geelen, Bert; Tack, Klaas; Tezcan Deniz Sabuncuoglu imec, Belgium	**E4.1 (P143) Thin IC Chip Pickup Process Risk Analysis via Experiments in conjunction with Numerical Approach** Tsai, Yi Hsuan (1); Shantaram, Sandeep (2); Lin, Yen Zhi (1); Chang, Yao Jung (1) 1: NXP Semiconductors, Taiwan; 2: NXP Semiconductors, TX, USA	**E5.1 (P208) Electromigration Study of Cu Pillar Interconnects in FC QFN Packaging under High Power devices** Tsai, Min-Yan (1); Kao, Chin-Li (1); Wang, Shan-Bo (1); Lin, Yung-Sheng (1); Liang, Chien-Lung (2) 1: Advanced Semiconductor Engineering, Taiwan; 2: National Taiwan University of Science and Technology, Taiwan	**E6.1 (P169) Artificial intelligence aided design for heterogeneous integration system in display** Huang, sixin (1); Zhou, Ziqing (2); Gao, Jiaying (2); Long, Haohui (2); Li, Jianhui (2) 1: Huawei Technologies Co., Ltd, China, People's Republic of; 2: Huawei Device Co., Ltd, China, People's Republic of	
4:40pm - 5:00pm	**E1.2 (P295) Development of Large RDL Interposer Package using RDL-first FOWLP Process** Ho, Soon Wee David; Soh, Siew Boon; Lau, Boon Long; Hsiao, Hsiang-Yao; Rao, Vempati Srinivasa Institute of Microelectronics, A*STAR, Singapore	**E2.2 (P330) Improvement in Wafer-to-Wafer Hybrid Bonding using Optimized Chemical Mechanical Planarization process for Cu Dishing** Khurana, Gaurav (1); Panchenko, Iuliana (1,2) 1: Institute of Electronic Packaging Technology, Technische Universitaet Dresden, Dresden, Germany; 2: All Silicon System Integration Dresden (ASSID), Fraunhofer Institute for Reliability and Microintegration IZM, Dresden, Germany	**E3.2 (P219) Development of Thick Sc0.2Al0.8N Film for MEMS Application** sharma, jaibir; Chen, Daniel Ssu-Han; Teo, Yong Shun; Liu, Patrick Peng Institute of Microelectronics, Singapore	**E4.2 (P154) Capillary Underfill Flow Simulation and Experimental Study for Solder Mask Opening and Trace Distribution** Lai, Jin Yuan (1); Yang, Shin Yueh (2); Lin, Kohan (3); Choi, Bongwoo (4); Ong, Yeow Chon (5); Ng, Hong Wan (6) 1: Micron Memory Taiwan, Co., Ltd.; 2: Micron Memory Taiwan, Co., Ltd.; 3: Micron Memory Taiwan, Co., Ltd.; 4: Micron Semiconductor Asia Operations Pte Ltd.; 5: Micron Semiconductor Asia Operations Pte Ltd.; 6: Micron Semiconductor Asia Operations Pte Ltd.	**E5.2 (P216) Detection of bonding voids in multi-tier stacks with SAM** Chen, Cong (1); Slabbekoorn, John (1); Bogdanowicz, Janusz (1); Moussa, Alain (1); Zhang, Boyao (1); Schleicher, Filip (1); Hoffrogge, Peter (2); Wiesler, Ingo (2); Phommahaxay, Alain (1); Beral, Christophe (1); Beyer, Gerald (1); Beyne, Eric (1); Charley, Anne-Laure (1); Leray, Philippe (1) 1: IMEC, Belgium; 2: PVA TePla Analytical Systems GmbH, Deutschordenstrasse 38, 73463 Westhausen, Germany	**E6.2 (P302) A NOVEL STRUCTURE OF MULTI MODE INTERFEROMETER WITH LOW LOSS** Li, Zhenyu (1); Li, Shuyi (2); Luo, Wei (2); Xu, Feng (1); Wen, Lee (1) 1: IME, A-STAR, SINGAPORE, Singapore; 2: EEE, NTU, SINGAPORE	
5:00pm - 5:20pm	**E1.3 (P314) Method of Triple Thin Film RDL Layers on 2.2D Substrate** Chen, Er-Hao (1); Hu, Dyi-Chung (1); Lee, Jeffrey ChangBing (2) 1: SiPlus Co., Ltd., Taiwan; 2: iST-Integrated Service Technology Inc., Taiwan	**E2.3 (P352) Evaluation of Low Temperature Inorganic Dielectric Materials for Hybrid Bonding Applications** Mishra, Dileep Kumar; Vasarla, Nagendra Sekhar; Chong, Ser Choong; Bhesetti, Chandra Rao; Chui, King Jien; Vempati, Srinivasa Rao Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR), Singapore	**E3.3 (P252) Systematic study of direct laser fabricated graphene resistor on FCCL** Hong, Priscilla (1); Goh, Zhen Ke (1); Qi, Xiaoying (2); Wan, Kebao (1) 1: DSBJ Pte. Ltd; 2: SIMTech, ASTAR, Singapore	**E4.3 (P160) Temperature-dependent creep characterization of lead-free solder alloys using nanoindentation** Dudash, Viktor (1,2); Machani, Kashi Vishwanath (2); Meier, Karsten (1); Geisler, Holm (2); Kuechenmeister, Frank (2); Wieland, Marcel (2); Bock, Karlheinz (1) 1: Institute of Electronic Packaging Technology, Technische Universität Dresden, Germany; 2: GlobalFoundries Dresden, Germany	**E5.3 (P102) Flip Chip CSP Package Integrity and Reliability Evaluation** Liu, Jinmei NXP, China, People's Republic of	**E6.3 (P346) Different nitrogen doping on multi-color fluorescent carbon dots synthesized from lychee exocarp for applications in LED down-conversion** Gong, Jingwei (1); Hou, LeiLei (3); Huang, Shuangwu (1); Ching, Yern Chee (2) 1: University of Shenzhen, China, People's Republic of; 2: University of Malaya, Malaysia; 3: Department of Catalytic Chemistry and Engineering & State key laboratory of fine chemicals, Dalian University of Technology, Dalian 116034,	
5:20pm - 5:40pm	**E1.4 (P356) Assembly Process Characterization of 3D Stacking of Heterogeneous Chiplets** Lim, Sharon Pei Siang; Lau, Boon Long; Chai, Tai Chong; Ye, Yong Liang Insitute of Microelevtronics, Singapore	**E2.4 (P365) Room Temperature Plasma-Enhanced Niobium-Niobium Wafer Bonding for 3D Integration of Superconducting Interconnects for Quantum Processing** Goh, Simon (1); Hemanth Kumar, Cheemalamarri Hemanth Kumar (1); Hu, Liangxing (2); Woon, Shervonne (1); Jaafar, Norhanani (1); Huang, Ding (3); Lau, Chit Siong (3); Kumar Karuppannan, Senthil (3); Li, Hongyu (1); Tan, Chuan Seng (1,2); Chui, King-Jien (1) 1: Institute of Microelectronics, Singapore; 2: Nanyang Technological University, Singapore; 3: Institute of Materials Research and Engineering, Singapore	**E3.4 (P279) Investigation of Void-free Chip-to Chip Bonding Methods for CMOS-MEMS Compatibility** Yeo, Yi Xuan; Wai, Eva Leong Ching; Chen, Daniel Ssu-Han; Chong, Ser Choong Institute of Microelectronics, A*STAR Research Entities, Singapore	**E4.4 (P229) Predicting Package Breaking Load of Thin BGA Packages Through Mechanical Modeling and Simulation** Talledo, Jefferson Sismundo STMicroelectronics, Philippines		**E6.4 (P362) Laser cavity electric connection line with SnAg solder for laser flip chip bonding** Chi, Ting Ta; Li, Zhenyu; Lim, Huiting Serene; Yoo, Jae Ok; Yu, Haitao; Sundaram, Arvind; Xu, Feng; Chong, Ser Choong; Lee, Wen Institute of Microelectronics, A*STAR (Agency for Science, Technology and Research), Singapore	

DAY 4: December 8, 2023 (Friday)

Venue	Canary 1	Canary 2	Oriole	Pelican	Kingfisher	Nightingale
08:30am -09:00am	**Invited Talk 7** New Innovation of Heterogeneous Integration in AI and ML Era (Jin Yang, Samsung)	**Invited Talk 8** Fluxless Bonding for Higher Density & Bandwidth Packaging (Steve Ng, KnS)	**Invited Talk 9** Signal and Power Integrity Performance of CoWoS-R in Chiplet Integration Applications (Chuei-Tang Wang, TSMC)	**Invited Talk 10** Fan-out Wafer Level Packaging Solutions for mmWave applications (Tanya Braun, Fraunhofer IZM)	**Invited Talk 11** Modeling and Characterization of Single Grain Solder Micro Bumps in Advanced Packaging (Jeffrey Suhling, Auburn Univ.)	**Invited Talk 12** Die-to-Wafer Hybrid Bonding to Addres Next-Gen Electronics Packaging Challenges (Avi Shantaram, Applied Materials)
09:00am -10:00am	Advanced Packaging Technologies II	Bumping Technologies II	Materials for Packaging	Assembly and Manufacturing Technology I	Mechanical Simulation & Characterization VI	Materials and Processing III
09:00am - 09:20am	**F1.1 (P386) Study on board-level reliability of passive components on ultra-high density PCB assemblies** Lv, Xiang; Shi, Hongbin; Li, Mengyuan Huawei Technologies Co., Ltd., China, People's Republic of	**F2.1 (P161) Microstructural and mechanical analysis of Cu/Sn/Cu microbump by doping Ni and Zn into Cu substrate** Huang, Pin-Wei; Lin, Ta-Wei; Duh, Jenq-Gong National Tsing Hua University, Taiwan	**F3.1 (P112) The Development of a Non-Conductive Die Attach Film for High-Reliability Applications** Bai, Jie (1); Do, Phuong (1); Kwak, Daniel (1); Chieng, Yuyuan (2); Hikita, Aya (2); Wu, Jie (2); Yun, Howard (1); Zhuo, Qizhuo (1); Peddi, Raj (2); Trichur, Ramachandran (1) 1: Henkel Corporation, Irvine, CA, USA; 2: Henkel Singapore Pte Ltd	**F4.1 (P185) Characterization of Differential TMV Vertical Interconnects to 50GHz with Double Side Measurement** Chang, Ting Wei (1); Ting, Jia Yunn (1); Wong, Chan Leong (1); Patel, Hamza (2) 1: NEXPERIA MALAYSIA SDN BHD, Malaysia; 2: NEXPERIA ,UK	**F5.1 (P170) TSV wafer warpage simulation by machine learning-based anisotropic equivalent modeling method** Wu, Xiaodong; Li, Chunlei; Ma, Shenling xiamen university, China, People's Republic of	**F6.1 (P1384) Characterizing Sub-micron 3D Defects from Intact Advanced Packages to Wafers Level Packaging using a Suite of Novel 3D X-ray Tools at Down to 0.3 µm Spatial Resolution** Lau, S.H.; Gelb, Jeff; Gul, Sheraz; Qin, Tianzu; Lewis, Sylvia; Yun, Wenbing Sigray Inc, United States of America
09:20am - 09:40am	**F1.2 (P176) Development of underground structure cover with slit for radio wave transmission** Yi, Yuantong (1); Tateishi, Eiichi (2); Kumagae, Takaya (2); Kai, Nobuhiro (2); Yamaguchi, Tatsuya (3); Kanaya, Haruichi (1) 1: Kyushu University, Japan; 2: HINODE Holdings Co., Ltd; 3: HINODE, Ltd.	**F2.2 (P241) Low temperature bonding of Cu/SnS8Bi/Cu with 5µm microbump for high temperature applications** Wu, Zih-You; Chen, Po-Yu; Duh, Jenq-Gong National Tsing Hua University, Taiwan	**F3.2 (P171) Pressure-less Copper sintering paste for Die attach application** Yao, Min (1); Han, Xuelian (1); Li, Hongyun (1); Ma, Li (1); Chen, Fen (1); Payne, Dean (2); Liu, Yan (3) 1: Indium Corporation of Suzhou, Suzhou, 215126, China; 2: Indium Corporation of Singapore, Singapore, 628908, Singapore; 3: Indium Corporation, New York, 13323, USA	**F4.2 (P186) Crack Package Improvement for the Small Diode Package by Optimizing the Mechanical Force at Final Test Process** Mohd Zali, Mohd Rozaini; Kow, Siew Ting; Ong, Yit Seng; Mohd Amin, Mohd Hadi Nexperia Malaysia Sdn Bhd, Malaysia	**F5.2 (P321) Experimental and Numerical Investigation of Die Shift in Large Panel Level Packaging** Luan, Jing En; Gu, Bin STMicroelectronics, Singapore	**F6.2 (P389) Ultrathin New Dielectric Interlayer Layer – Enhancer for TEOS-TEOS Bond Strength at Low Thermal Budget for C2W and W2W Bonding Applications.** Cheemalamarri, Hemanth Kumar; Hou Jang, Steven Lee; Ji, Hong Miao; Venkataraman, Nandini; Bhesetti, Chandra Rao; Chui, King Jien; Vempati, Srinivasa Rao; Singh, Navab Institute of Microelectronics, A*STAR, Singapore
09:40am - 10:00am	**F1.3 (P366) Influence of Parasitic Power Loop Inductance on Switch Performance in GaN HEMT** Wu, Ping; Ma, Chuangwei; Qiu, Yiou; Qian, Xin; Wang, Liancheng; Zhu, Wenhui Central South University, China, People's Republic of China	**F2.3 (P248) Investigation of Two-Stage Ag-Sintering Processes for the Die Attach of Power Devices** Sumkötter, Dominik (1); Wollschläger, Mario (1); Köhler, Marius (1); Lawniczak, Marcel (2); Weickmann, Johannes (1); Besendörfer, Kurt-Georg (2); Heuck, Nicolas (1) 1: Hamm-Lippstadt University of Applied Sciences, Germany; 2: Semikron-Danfoss, Nuremberg, Germany	**F3.3 (P240) Intra Die Super Power Pads Bonding for IR Voltage Drop Reduction in Automotive SoCs** Sharma, Ajay Kumar; Kumari, Aanchal; Bhooshan, Rishi; Jain, Shreyans NXP Semiconductors pvt ltd, India	**F4.3 (P218) uPoP- Innovative Solution for Mobile Memory Package** Li, Brian; Sun, Isaac; Shi, Stephen; Zhu, James; Pan, Tao; Quan, Changhao; Ahn, Charles Changxin memory technical, China, People's Republic of	**F5.3 (304) Virtual Design of Experiment Methodology for Package Design Robustness** Duca, Roseanne STMicroelectronics, Malta	**F6.3 (384) Realizing ultra-thin high reliability storage devices with large capacity by package and PCB collaborative design** Shi, Hongbin; Yang, Chao; Zhang, Jianrui Huawei Technologies Co., Ltd
10:00am - 10:30am	Coffee/Tea Break (Grand Ballroom Foyer)					
Venue	Canary 1	Canary 2	Oriole	Pelican	Kingfisher	Nightingale
10:30am -11:50am	Thermal Management II	Interconnection Technologies	Materials and Processing IV	Assembly and Manufacturing Technology II	Failure Analysis II	TSV/Wafer Level Packaging
10:30am - 10:50am	**G1.1 (P381) A high flow rate piezoelectric micropump for miniature liquid cooling system** Fan, Yiwen; Zhang, Xinfeng; Xing, Guanying; Xiang, Linyi; Hu, Run; Luo, Xiaobing Huazhong Univeisity of Science and Technology, China, People's Republic of	**G2.1 (164) Eliminating Preferred orientation and Refining Grain Size with Ni doping in Cu/Sn-3.0Ag-0.5Cu/Cu TLP Bonding under isothermal aging treatment** Chao, Chen-Sung; Chen, Zi-Xu; Duh, Jenq-Gong National Tsing Hua University, Taiwan	**G3.1 (P123) Dry Film Resist with Four Key Technologies to Achieve L/S=1/1µm Pattern** Togasaki, Kei; Toda, Natsuki; Yoshihara, Kensuke; Kaguchi, Yosuke; Funai, Kanako; Onozeki, Hitoshi; Iwashita, Kenichi Resonac Corporation., Japan	**G4.1 (P230) Integration of plasma dicing in the collective die to wafer hybrid bonding** Suhard, Samuel (1); Kennes, Koen (1); Bex, Pieter (1); Sleicher, Filip (2); Walsby, Edward (2); Jourdain, Anne (1); Beyer, Gerald (1); Beyne, Eric (1) 1: IMEC, Belgium; 2: KLA, UK	**G5.1 (P243) A Novel Burn-Out Failure of Microbump During Electromigration** Yao, Yifan (1); An, Yuxuan (2); Tu, King-Ning (1,2,3); Liu, Yingxia (2) 1: Department of Materials Science and Engineering, City University of Hong Kong, Hong Kong S.A.R. (China); 2: Department of Systems Engineering, City University of Hong Kong, Hong Kong S.A.R. (China); 3: Department of Electrical Engineering, City University of Hong Kong, Hong Kong S.A.R. (China)	**G6.1 (P288) Demonstration and Challenges of Through Si Interposer (TSI) with 5-layer Frontside Cu metal and 2-layer backside Cu RDL** Tseng, Ya-Ching; Chui, King-Jien Institute of Microelectronics Agency for Science, Technology and Research (A*STAR), Singapore
10:50am - 11:10am	**G1.2 (P122) Development of crossflow manifold for two-phase liquid cooling of 3D ICs via 3D printing** Feng, Huicheng; Tang, Gongyue; Zhang, Xiaowu; Lau, Boon Long; Jong, Ming Chinq; Au, Keng Yuen Jason; Ong, Jun Wei Javier; Chui, King Jien; Li, Jun; Li, Hongying; Le, Duc Vinh; Lou, Jing A*STAR, Singapore	**G2.2 (P181) Laser Direct Structuring (LDS) for enhanced QFN package** Catalano, Guendalina; Cecchetto, Luca; Sanna, Aurora; Verardi, Erwin; Villa, Riccardo; Vitello, Dario STMicroeltronics, Italy	**G3.2 (P163) Process development, microstructure and electronic resistance on green laser induced graphene from polyimide** Liu, Shibo (1); Qi, Xiaoying (2); Chew, Youxiang (1); Goh, Min Hao (2); Cheng, Xin Wei (1); Ng, Fern Lan (2) 1: Advanced Remanufacturing and Technology Centre / Agency for Science, Technology and Research, Singapore 637143; 2: Singapore Institute of Manufacturing Technology / Agency for Science, Technology and Research, Singapore 636732	**G4.2 (P281) Cu and barrier CMP process development with fine 1µm Cu bond pad and 2.5 µm pitch for Wafer-to-wafer HB** Chaki Roy, Sangita; Gim Guan, Chen; Venkataraman, Nandini; Lee, Wen; Singh, Navab Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR), Singapore, Singapore	**G5.2 (P249) Failure Mode Evaluation of QFP Package Interconnect Structure under Random Vibrations** Shimamura, Nozomi Yokohama National University, Japan	**G6.2 (P127) Through glass vias fabrication using ultrasonic machining and electroless deposition** Pawar, Karan; Pandey, Harsh; Dixit, Pradeep Indian Institute of Technology Bombay, India
11:10am - 11:30am	**G1.3 (P278) Design of liquid cooling cold plate for high performance electric traction module on two-wheeler EV** He, Bin (1); Saha, Jaydeep (2); Tang, Gongyue (1); Panda, Sanjib Kumar (2) 1: Institute of Microelectronics (IME), Agency for Science, Technology & Research (A*STAR), Singapore; 2: Department of Electrical & Computer Engineering (ECE), National University of Singapore (NUS)	**G2.3 (P244) Fine Pitch Integration (<5 µm) and Challenges for Die-to-Wafer assembly using Hybrid Bonding** Dubey, Vikas; Wünsch, Dirk; Gottfried, Knut; Wiemer, Maik Fraunhofer ENAS, Germany	**G3.3 (P202) Development of UV Curable Wafer Back Side Protection-Film - IR Shielding Type-** Yamashita, Shigeyuki; Kobashi, Rikiya; Sato, Soki Lintec Corporation, Japan	**G4.3 (P337) Effect of Scribe Line Metal Layout on Wafer Saw Top Edge Chipping for Silicon Power Devices** Gambino, Jeff (1); Barbosa, Ronald (2) 1: Onsemi, United States of America; 2: Onsemi, Philippines	**G5.3 (P306) Lock-in Thermography judgment for short/leakage/high resistance defects in advanced Fan-Out packages** Lin, Yu-Ting Advanced Semiconductor Engineering, Taiwan	**G6.3 (P359) RF Modelling of for Through SiC Vias and Fabrication of SiC based Interposer** Mackowiak, Piotr (1); Köszegi, Julia-Marie (1); Schiffer, Michael (1); Schneider-Ramelow, Martin (2) 1: Fraunhofer IZM, Germany; 2: Technische Universität Berlin, Germany
11:30am - 11:50am	**G1.4 (P225) Immediate thermal performance evaluation of the power module structures under real operating conditions** Sudo, Tomoya (1); Hiraoka, Gakuto (1); Yu, Qiang (1); Liu, Wei (2); Muraoka, Mitsutoshi (2); Komatsu, Yuji (2) 1: Yokohama National University, Japan; 2: ZF Japan Co., Ltd., Japan	**G2.4 (P307) A Conceptional Study towards Developing a Novel Copper Top-Side-Interconnection in Power Electronics using Additive Manufacturing** Ockel, Manuela; Sippel, Marcel; Franke, Jörg Friedrich-Alexander-University Erlangen-Nuremberg, Germany	**G3.4 (Invited Talk) Die to Wafer (D2W) Hybrid Bonding for Advanced Heterogeneous Integration** Jonathan Abdilla BESI	**G4.4 (P343) Comparative Analysis of Laser Parameters effect on Laser Splash Performance in DFL7361 Stealth Dicing Tools** George, Nathaniel Simon; Harish Shah, Ankur; Tanola, Rommel; Lu, Jane; Sim, Chris; Singh, Harry Micron Semiconductor Asia Pte Ltd, Singapore	**G5.4 (P317) A Board Level Vibration Test Method for Electronic Industry Application** Lee, Jeffrey ChangBing (1); Xie, Dongji (2); Khaldarov, Valeriy (3) 1: iST-Integrated Service Technology Inc., Taiwan; 2: Nvidia Corporation; 3: ASONIKA, LLC	**G6.4 (P221) Evolution of Nano-notches on the Surface of SiC with Different Crystal Forms during Cutting in the Water Environment** Zhou, Yuqi; Lv, Weishan; Zhu, Fulong Huazhong University of science and technology, China, People's Republic of
Venue	Canary 1 / Canary 2		Grand Ballroom foyer			
11:50am - 1:20pm	**Young Professionals' Event**		Standing lunch in foyer			
Venue	Canary 1 / Canary 2		Oriole	Pelican	Kingfisher	
1:20pm -2:40pm	**HIR workshop**		Materials and Processing V	Electrical Simulations & Characterization I	Packaging Technologies & Solutions I	
1:20pm - 1:40pm			**H3.1 (P255) GuardCoatTM Applications to Eliminate Dicing Edge Chip-out** Moore, John Cleaon; Gray, Allison; Iglesias, Franco Daetec LLC, United States of America	**H4.1 (P121) Time Interval Error(TIE)-based SI Design and Characterization of DDR5 Data Strobe Signaling** Park, Shinyoung (1); Arjun Huddar, Vinod (2) 1: Rambus Inc., United States of America; 2: Rambus Inc., India	**H5.1 (P334) Qualification of High Coplanarity Large Package for Advanced Computing and AI** Murthy, Balan (1); Kanaran, Sreedharan Kelappen (1); Ramachandran, Premkumar (1); Michael, Bernard Raj (1); Gunasekaran, Munisshwaran (1); Refai-Ahmed, Gamal (2); Karunakaran, Nagadeven (2); Baharom, Muhammad Afiq (2) 1: Flex; 2: AMD	
1:40pm - 2:00pm	1:20 pm - 1:25 pm Welcome & Agenda Review by William (Bill) Chen and Mahajan 1:25 pm - 2:00 pm Keynote Address by Choon Khoon Lim, Senior VP, ASM Pacific 2:00 pm - 2:10 pm HIR Briefing by William Chen 2:10 pm – 2:20 pm 2D-3D & interconnect by Ravi Mahajan 2:20 pm - 2:30 pm Mobile by Bonson Chan 2:30 pm - 2:40 pm Modelling & Simulation by Chris Bailey		**H3.2 (P260) High Precision Wafer Thinning Using Ultra-low-TTV Glass Carrier and Novel Temporary Bonding** Zhang, Jay Corning Incorporated, United States of America	**H4.2 (P134) RDL Routing Optimisation using the variation of trace width and length to Equalise trace parasitics.** Shaw, Mark (1); Papic, Vladimir (2) 1: STMicroelectronics Srl, Italy; 2: Cadence Design Systems Inc	**H5.2 (P101) Reliability Assessment of Gripper Socket Under Post-Silicon Validation Conditions** Al-Momani, Emad (1); Harb, Shadi (2) 1: Al Hussein Technical University, Jordan; 2: Intel Corporation, United States of America	
2:00pm - 2:20pm	1:20 pm - 1:25 pm Welcome & Agenda Review by William (Bill) Chen and Mahajan 1:25 pm - 2:00 pm Keynote Address by Choon Khoon Lim, Senior VP, ASM Pacific 2:00 pm - 2:10 pm HIR Briefing by William Chen 2:20 pm - 2:30 pm Mobile by Bonson Chan 2:30 pm - 2:40 pm Modelling & Simulation by Chris Bailey		**H3.3 (P211) Investigation of Immersion Alignment Mark Signal and Alignment Success Rate for Flat Optics with Aperture on Chip** Tew, Chin Khang; Tobing, Landobasa Y. M.; Yoo, Jae Ok; Singh, Navab A*STAR - Institute of Microelectronics (IME), Singapore	**H4.4 (P215) Design of Four-Way Multiplexer with Integrated Lumped Elements for Qubit Characterization** Shanmugam Bhaskar, Vignesh; Dragos Rotaru, Mihai Agency for Science, Technology and Research, Singapore	**H5.3 (P340) Assembly of Thin Micro-Chiplets using Laser-Induced Forward Transfer** Kannojia, Harindra Kumar (1,2); Van Steenberge, Geert (1,2) 1: Center for Microsystem Technology (CMST), IMEC, Belgium; 2: Ghent University, Belgium	
2:20pm - 2:40pm			**H3.4 (P308) Various dicing approaches for Silicon Carbide Wafers** Jeon, YuJin; Na, SeokHo; Gim, MinSoo; Bae, JoHyun; Ryu, DongSu; Park, DongJoo; Park, KyungRok Amkor Technology, Korea, Republic of (South Korea)	**I4.2 (P327) Analysis of the influences of PCB process tolerances and assembly tolerances on 60 GHz radar sensor for Radar toolkit** Tschoban, Christian Fraunhofer IZM, Germany	**H5.4 (P246) Effect of cohesive behaviour and residual stress on the indentation response of elastoplastic film/substrate structure** Li, Jiao; Long, Xu Northwestern Polytechnical University, Xi;an, People's Republic of China	
2:40pm - 3:00pm	Coffee/Tea Break (Grand Ballroom Foyer)					
3:00pm - 4:20pm	**HIR workshop**		Materials and Processing VI	Packaging Technologies & Solutions II		
3:00pm - 3:20pm			**I3.1 (P336) Characterization and Analysis of High Efficiency in Aqueous-Based Flux Cleaning Process for High Voltage Power Device Packages** Ramalingam, Vegneswary; Morales, Leonardo Samson Nexperia Malaysia Sdn Bhd	**I4.1 (P376) Opto-Mechanical System design for characterizing multiple channel free space optical interconnect components** Penumaka, Shushil Kumar; Mattur, Chandramohan Raghuveer; Pamidigantam, Ramana; Yeluripati, Rohin kumar LightSpeed Photonics Private Limited, Singapore		
3:20pm - 3:40pm	3:00 pm - 3:10 pm Co-Design by Jose Schutt-Aine 3:10 pm - 3:20 pm Supply Chain by Kitty Pearsall 3:20 pm - 3:30 pm Integrated Power Electronics by Patrick McClusky 3:30 pm - 3:40 pm SiP & Module by Erik Jung 3:40 pm - 3:50 pm Test by Fisher Zhang 3:50 pm - 4:00 pm HIR Workshop Wrap-Up by William Chen & Ravi Mahajan		**I3.2 (P338) In-Package Relative Humidity Sensor with Multi-Width Interdigital Electrodes Towards Enhanced Sensitivity for Characterization of Packaging Encapsulation Materials** Sattari, Romina; van Zeijl, Henk; Zhang, GuoQi Delft university of technology, Netherlands, The	**I4.3 (P107) Simulation study of the magnetic material patterning on the high frequency planer inductor in 5G device application** Masuda, Seiya; Ohtsu, Akihiko; Miyata, Tetsushi; Suzuki, Hiroyuki; Takahashi, Hidenori FUJIFILM Corporation, Japan		
3:40pm - 4:00pm			**I3.3 (P380) The path traversal method for the orientation information of fillers in composites** Zhang, Xinfeng; Fan, Yiwen; Yang, Xuan; Xiang, Linyi; Xing, Guanying; Hu, Run; Luo, Xiaobing State Key Laboratory of Combustion, School of Energy and Power Engineering, Huazhong University of Science and Technology, Wuhan 430074, China.	**I5.2 (P367) Research on technology and isothermal aging of double sided module convex interconnect** Qiu, Yiou; Chen, Huapeng; Wu, Ping; Qian, Xin; Wang, Liancheng; Zhu, Wenhui Central South University, China, People's Republic of China		
4:00pm - 4:20pm			**I3.4 (P214) Wire loop characterization for wire sweep reduction** Leone, Federico; Caglio, Carolina; Viviani, Fulvio; Villa, Riccardo STMicroelectronics, Italy	**I5.3 (P193) Adhesive Fracture Analysis of Die Attach Film-Laminated Tape by Peel Test** Zhao, Facheng; Yang, Kai; Cheng, Yu Seng Infineon Technologies Asia Pacific Pte Ltd, Singapore		
Venue	Grand Ballroom Foyer					
4:30pm - 5:00pm	Closing Ceremony and Lucky Draw					