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1	119	Application of Auger Electron Spectroscopy in Copper oxide Failure in Electronics Packaging Zhao, Yanfei (1); Zhu, Lei (2); Hua, Younan (2); Li, Xiaomin (2) <i>1: Wintech-Nano (Suzhou) Co., Ltd., China, People's Republic of China; 2: Wintech Nano-Technology Services Pte Ltd, Singapore</i>
2	138	Chip-Package Interaction: A Case Study Applied To A Mature Technology Node Chua, Eng Chye (1); Kuechenmeister, Frank (2); Geisler, Holm (2); Vishwanath Machani, Kashi (2); Yap, Hin Kiong (1) <i>1: Globalfoundries Singapore Pte Ltd, Singapore; 2: GlobalFoundries Dresden LLC & Co. KG, Germany</i>
3	146	Effects of temperature and electrical bias on Cu-Al IMCs growth Liao, Lois Jinzhi <i>WinTech Nano-Technology Services Pte. Ltd., Singapore</i>
4	150	Crazing of photoimageable dielectric (PID) in Fan-Out Panel Level Packaging (FOPLP) Yu, Yeonseop (1); Lee, Sunguk (1); Jeon, Jongmyeong (2); Kim, Miyang (2) <i>1: Samsung Electronics, Korea, Republic of (South Korea); 2: Samsung Electro-Mechanics, Korea, Republic of (South Korea)</i>
5	152	Assessment of Delamination Risk During Sawing Process by Simulation Yahaya, Khairul Ikhsan (1); Kong, Chen Wei (1); Leung, Max (2) <i>1: Nexperia Malaysia Sdn. Bhd., Malaysia; 2: Nexperia Hong Kong Limited</i>
6	167	Package Design Optimization of Thin Mold Double Side System in Package (DS-SIP) Yen, Freedman <i>SPIL, Taiwan</i>
7	195	Acceptance Criteria for Good Solder Joint Reliability on Wafer Level Chip Scale Package (WLCSP) at Component Level Periasamy, Subashini; Supramaniam, Saraswathy; Abdullah, Muhammad Nurhisham; Balasupramaniam, Selvakumar <i>Nexperia Malaysia Sdn Bhd, Malaysia</i>
8	200	An Extensive Study of the Effects of Packaging Structure and Material Properties on Reliability of Advanced Packages by Charactering Stress Singularities at Interface Corners Lyu, Guang-Chao; Chen, Bin; Zhou, Min-Bo; Ke, Chang-Bo; Zhang, Xin-Ping <i>South China University of Technology, China, People's Republic of</i>
9	205	Life assessment of Micro-via used in thin Printed Circuit Board under Thermal Cycling loads & influence of selected design parameters Kumar, Vinay; Bhadri, Shrikant <i>APTIV, India</i>
10	212	Nanoindentation characterization of sintered porous Cu nanoparticles used in power electronics packaging – A molecular dynamics simulation study Hu, Dong (1); Li, Zichuan (1); Fan, Jiajie (1,2,3); Zhang, Guoqi (1) <i>1: EEMCS Faculty, Delft University of Technology, The Netherlands; 2: Institute of Future Lighting, Academy for Engineering & Technology; Shanghai Engineering Technology Research Center for SiC Power Device,, Fudan University, China; 3: Research Institute of Fudan University in Ningbo, China</i>
11	223	Silicon measurement, Debug & Root Cause Analysis for Crystal Oscillator Jitter degradation Bhooshan, Rishi; Tiwari, Swapnil <i>NXP Semiconductor Inc</i>
12	226	Parasitic Surface Conduction Effect of TSV on Interconnection Performance in RF SOI for 2.5D Integration Zhou, Lin; Lim, Teck Guan; Wu, Jiaqi; Xu, Feng; Jong, Ming Ching; Ng, Yong Chyn <i>Institute of Microelectronics, Singapore</i>
13	228	Optimizing Package Power Integrity: A Comparative Study of Multiple Techniques and Approaches Ibeni, Ahmad Afiq; Lee, Wai Ling; Tan, Yee Wei; Shahneer, Anis Shazlin <i>Intel Microelectronics (M) Sdn. Bhd., Malaysia</i>
14	229	Predicting Package Breaking Load of Thin BGA Packages Through Mechanical Modeling and Simulation Talledo, Jefferson Sismundo <i>STMicroelectronics, Philippines</i>
15	300	A Novel Silicon Crystal Defect Detection Method Using Cross-sectional Samples Hua, Younan; LIAO, Lois; Zhang, Linhua <i>WinTech Nano-Technology Services Pte. Ltd., Singapore</i>
16	310	Integrated heat management in the reticle masking module on the LITEQ 500 projection stepper Loktev, Mikhail; de Boeij, Jeroen; Misat, Sylvain; van der Stam, Michiel <i>Kulicke & Soffa Liteq BV, the Netherlands</i>
17	208	An Electromigration Study of Cu Pillar Interconnects in Flip-chip QFN Packaging under Extreme Conditions for High-power Applications Tsai, Min-Yan (1); Kao, Chin-Li (1); Wang, Shan-Bo (1); Lin, Yung-Sheng (1); Liang, Chien-Lung (2) <i>1: Advanced Semiconductor Engineering, Taiwan; 2: National Taiwan University of Science and Technology, Taiwan</i>