

DAY 1: December 3, 2024 (Tuesday)	
08:00am - 08:55am	Registration
Venue	Grand Ballroom (Level 4)
09:00am - 09:15am	Opening Ceremony
09:15am - 10:00am	<p><b>Calvin Cheung</b>, VP, ASE Inc</p> <p><b>KEYNOTE: Advanced Packaging for AI Performance and Power Efficiency</b></p>
10:00am - 10:45am	<p><b>Glenn G. Daves</b>, Senior VP, NXP Semiconductors</p> <p><b>KEYNOTE: Packaging at the Emerging Edge</b></p>
10:45am - 11:00am	Coffee/Tea Break (Grand Ballroom Foyer)
11:00am - 12:30pm	Panel Session: <b>Enhancing Southeast Asia's Importance in the Global Semiconductor Supply Chain</b> (Moderator: Keat Yap, Kearney)
	Panelist: Andrew Goh (Lam Research), Chan Pin Chong (Kulicke and Soffa), Soon Lim (SSMC), Bertrand Stoltz (STMicroelectronics) and Wee Seng Ang (SSIA)
12:30pm - 1:30pm	Lunch @ Grand Ballroom Foyer (Level 4)
1:15pm - 1:30pm	<b>Sponsor Appreciation @ Grand Ballroom (Level 4)</b>
1:30pm - 2:15pm	<p><b>Dr Yu-Po Wang</b>, VP, Siliconware Precision Industries Co., Ltd.</p> <p><b>KEYNOTE: Breaking Boundaries of IC Packaging through Innovative Integration Technology</b></p>
2:15pm - 3:00pm	<p><b>Tim Olson</b>, CEO, Deca Technologies</p> <p><b>KEYNOTE: Tectonic Forces Shaping the Future of the Semiconductor Industry</b></p>
3:00pm - 3:45pm	<p><b>Dr Devan Iyer</b>, Chief Strategist (Advanced Packaging), IPC International</p> <p><b>KEYNOTE: Advanced Packaging-Customization Trends and Standardization Opportunities</b></p>
3:45pm - 4:00pm	Tea Break (Grand Ballroom Foyer)
4:00pm - 5:30pm	<p>Panel Session: <b>The Role of Co-Packaged Optics in Advancing AI Technologies</b> (Moderator: Matt Kelly/Dr Devan Iyer, IPC International Inc.)</p> <p>Panelist: Dr Masaki Kato (Marvell), Dr Torseten Wipiejewki (Huawei), Prof Subramanian S Iyer (UCLA), Calvin Cheung (ASE) and PV Ramana (Lighspeed Photonics)</p>
6:00pm - 8:00pm	<b>VIP Dinner (by invitation only)</b>

## DAY 2: December 4, 2024 (Wednesday)

## Exhibition at Waterfront Foyer from 10:30am to 5:30pm (Level 2)

Venue	Veranda I	Veranda II	Veranda III	Riverfront I	Riverfront II	Riverfront III
08:45am - 10:30am	PDC1	PDC2	PDC3	PDC4	PDC5	PDC6
	Chiplet, Heterogeneous Integration and Co-Packaged Optics	Photonic Technologies for Communication, Sensing and Displays	Wafer Bonding for Advanced Packaging Applications	Current and Future Challenges and Solutions in AI & HPC	Mechanics and Reliability of Lead-Free Solders Joints	FA of Advanced Packages: Fundamental, Skills, Philosophy & Case Studies
	Dr John H. Lau, Unimicron Technology Corporation	Dr Torseten Wipiejewski, Huawei	Dr Viorel Dragoi, EV Group	Dr Refai-Ahmed Gamal, AMD	Professor Jeff Suhling, Auburn University	Dr Yong-Fen Hsieh, MA-Tek
10:30am - 11:00am	Tea Break & Exhibition (Waterfront Ballroom Foyer)					
11:00am - 12:30pm	PDC1 (cont'd)	PDC2 (cont'd)	PDC3 (cont'd)	PDC4 (cont'd)	PDC5 (cont'd)	PDC6 (cont'd)
12:30pm - 2:00pm	<b>EPS Luncheon @ Waterfront Ballroom Level 2</b> (Including the presentation of OC Appreciation Certificates and Student Travel Grant Awards)					
2:00pm - 2:45pm	<b>Professor Subramanian S. Iyer</b> , Distinguished Professor, UCLA  <b>KEYNOTE: Strategic Directions for Electronics Packaging</b>					
2:45pm - 3:15pm	<b>Dr Victor Zhirnov</b> , Semiconductor Research Corporation (SRC)  <b>TECHNOLOGY TALK: New Roadmap for Microelectronics: Charting the Semiconductor Industry's Path Over the Next 5, 10, and 20 Years</b>					
3:15pm - 4:15pm	R10 Chapter Chairs' Meeting	Interactive Poster Presentation I / Exhibition / Coffee Break @ Waterfront foyer (Level 2)				
4:15pm - 6:15pm	Sponsor Presentations at Riverfront I, II and III – Plus Quiz & Prizes!					
6:15pm - 6:30pm	Transport to EPTC Banquet Dinner					
6:30pm - 9:00pm	EPTC Banquet Dinner, RedDot BrewHouse @ Dempsey Hill					

**DAY 3: December 5, 2024 (Thursday AM)**  
**Exhibition at Waterfront Foyer from 9:00am to 5:30pm (Level 2)**

Venue	Veranda I	Veranda II	Veranda III	Riverfront I	Riverfront II	Riverfront III
09:00am -09:30am	<b>Invited Talk 1: James Papanu, Tokyo Electron Limited</b> D2W Hybrid & Fusion Bonding to Enable Advanced Packaging	<b>Invited Talk 2: Tan Yik-Yee, Yole Group</b> Glass Core Substrate Market and Opportunity	<b>Invited Talk 3: Winston Zhang, Novark Technologies</b> Pulsating Heat Pipes for Electronics Cooling	<b>Invited Talk 4: Chan Pin Chong, Kulicic &amp; Soffa</b> Fluxless TCB for Chiplet Integration	<b>Invited Talk 5: Chai Tai Chong, IME</b> RDL-First Interposer Technology for Next Generation Advanced Packaging	<b>Invited Talk 6: Hardik Kabaria, Vinci4D</b> Towards AI-Assisted Design of Thermal Management Strategies
09:30am -10:30am	<b>A1. Hybrid and Fusion Bonding 1</b>	<b>A2. Wafer Processing and Characterization</b>	<b>A3. Emerging Technologies I</b>	<b>A4. Advanced Packaging 1</b>	<b>A5. TSV and Wafer Level Packaging 1</b>	<b>A6. Thermal Management and Characterization 1</b>
09:30am - 09:50am	A1.1 (P1187) Improved Edge Detection Algorithm for Blurred Alignment Marks in Hybrid Bonding  <i>Sugiura, Takamasa (1); Nagatomo, Daisuke (1); Kajinami, Masato (1); Ueyama, Shiro (1); Tokumiya, Takahiro (1); Oh, Seungyeol (2); Ahn, Sungmin (2); Choi, Euisun (2); Woo, Siwoong (2); Lee, Hyunjin (2); Lee, Byungjoon (2); Rhee, Minwoo Daniel (2)</i>  Samsung Japan Corporation (1)	A2.1 (P1412) Comprehensive Die Strengths Comparisons for Glass using Different Singulation Methods  <i>Wei, Frank</i>  DISCO Corporation, USA	A3.1 (P1367) Trade-off between Chiplet Dimensions and Packaging Parameters for Optimal cost-performance for Chiplet Based Heterogenous Integration  <i>Sahoo, Krutikesh (1); Zhai, Max (2); Iyer, Subramanian (1)</i>  UCLA, USA (1)	A4.1 (P1262) Dual Damascene process for 500nm RDL using High Resolution Photosensitive Polymer  <i>Gerets, Carine Helena; Pinho, Nelson; Tseng, Wen Hung; Paulus, Tinneke; Labyedh, Nouha; Beyer, Gerald; Miller, Andy; Beyne, Eric</i>  IMEC, Belgium	A5.1 (P1344) Accelerating Overlay Error Optimization in Fine-Pitch Wafer-to-Wafer Hybrid Bonding through ML  <i>James, Ashish (1); Venkataraman, Nandini (2); Miao, Ji Hong (2); Singh, Navab (2); Li, Xiaoli (1)</i>  Institute for Infocomm Research, Singapore (1)	A6.1 (P1136) Thermal Design and Analysis of a Flip-Chip GaN-on-SiC HEMT  <i>Feng, Huicheng; Zhou, Lin; Tang, Gongyue; Wai, Eva Leong Ching; Lim, Teck Guan</i>  Institute of Microelectronics, Singapore
09:50am - 10:10am	A1.2 (P1195) Post-CMP Clean Optimization for SiCN Hybrid Bonding Applications  <i>Ji, Hongmiao (1); LEE, Chaeun (1); TEE, Soon Fong (1); TEO, Wei Jie (1); TAN, Gee Oon (1); Venkataraman, Nandini (1); Lianto, Prayudi (2); TAN, Avery (2); LIE, Joselyn (2); SUM, Darren (2); SEOW, Kevan (2); CHEOK, Kelvin (2); CHONG, Hoi Jin (2); TAMBOLI, Dnyanesh (3); TEO, Melvin (3)</i>  Institute of Microelectronics, Singapore (1)	A2.2 (P1388) 200mm Reconstituted Wafer for Fan-out of Microfluidics and CMOS Electronics  <i>Wei, Wei; Zhang, Lei; Tobback, Bert; Visker, Jakob; Stakenborg, Tim; Karve, Gauri; Tezcan, Deniz Sabuncuoglu</i>  IMEC, Belgium	A3.2 (P1253) Feasibility and Performance of Fully Additive Manufactured Light Bulbs  <i>Ankenbrand, Markus; Piechulek, Niklas; Franke, Jörg</i>  Friedrich-Alexander Universität Erlangen Nürnberg, Germany	A4.2 (P1342) ECC-based Flux Cleaning Monitoring for Improved Reliability in Advanced Packaging Products  <i>Wang, Yusheng; Huang, Baron; Lin, Wen-Yi; Zou, Zhihua; Kuo, Chien-Li</i>  TSMC, Taiwan	A5.2 (P1373) Study of Direct Copper Electroplating on Ruthenium Seed Layer for TSV Processes at 300mm Wafer Level  <i>Tran, Van Nhat Anh; Venkataraman, Nandini; Tseng, Ya-Ching; Chen, Zhixian</i>  Institute of Microelectronics, Singapore	A6.2 (P1163) Silicon-Based Micro-Fluid Cooler Package Integration for High Performance Computing  <i>Han, Yong; Tang, Gongyue; Lau, Boon Long</i>  Institute of Microelectronics, Singapore
10:10am - 10:30am	A1.3 (P1369) Maximizing Productivity through Bonding Sequence Optimization in the Chip on Wafer Process  <i>Kim, Junsang (1); Yun, Hyeonjun (1); Kang, Mingu (1); Cho, Kwanghyun (1); Cho, Hansung (1); Kim, Yunha (1); Moon, Bumki (1); Rhee, Minwoo (1); Jung, Youngseok (2); Lee, Byungjoon (1); Kwon, Ohwoon (2); Joung, Geewoong (2); Kim, Jisu (1); Lee, Jungchul (2)</i>  Samsung Electronics, South Korea (1)	A2.3 (P1332) Diffraction Alignment Sensor and Mark Design Optimization to Enable Fine Overlay Accuracy for 50 um Thick Si Bonded to Glass  <i>Tamadon, Amir-Hosseini (1); Jadli, Imene (1); Suhard, Samuel (1); Jourdain, Anne (1); Hsu, Alex (2); Schaap, Charles (2); De Poortere, Etienne (2); Miller, Andy (1); Kennes, Koen (1); Blanco, Victor (1)</i>  IMEC, Belgium (1); ASML (2)	A3.3 (P1377) Innovations and Challenges in Laser Direct Structured Mechatronic Integrated Devices for Aviation  <i>Piechulek, Niklas; Ankenbrand, Markus; Xu, Lei; Fröhlich, Jan; Nguyen, Huong Giang; Franke, Jörg</i>  Lehrstuhl für Fertigungsautomatisierung und Produktionssystematik	A4.3 (P1256) Deflusing in Advanced Packaging: Critical Process Considerations and Solutions  <i>Parthasarathy, Ravi</i>  ZESTRON Americas	A5.3 (P1227) Utilizing Ensemble Learning on Small Database for Predicting the Reliability Life of Wafer-Level Packaging  <i>Su, Qinghua (1); Yuan, Cadmus (2); Chiang, Kuo-Ning (1)</i>  National Tsing Hua University, Taiwan (1)	A6.3 (P1103) Power Management IC device Efficiency & Thermal Study  <i>Ge, Garry; Xu, L.Q.; Zhang, Bruce; Zeng, Dennis</i>  NXP Semiconductor Company, China
10:30am - 10:45am	<b>Tea Break &amp; Exhibition (Waterfront Ballroom Foyer)</b>					
10:45am - 11:45am	<b>B1. Hybrid and Fusion Bonding 2</b>	<b>B2. Interconnection Technologies 1</b>	<b>B3. Thermal Interface Materials</b>	<b>B4. Advanced Packaging 2</b>	<b>B5. Assembly and Manufacturing Technology 1</b>	<b>B6. Thermal Management and Characterization 2</b>
10:45am - 11:05am	B1.1 (P1211) Next Generation of Thermo Compression Bonding Equipment  <i>Abdilla, Jonathan</i>  Besli, Austria	B2.1 (P1221) Study of Solder Bump and Joint Standoff Height Profiles Using Empirical and Numerical Methods  <i>Wang, Yifan; Yeo, Alfred; CHAN, Kai Chong</i>  STATS ChipPac, Singapore	B3.1 (P1113) Evaluation of TIM Cross-Sectioning Methods on Lidded High-Performance Microprocessors  <i>Neo, Shao Ming; Song, Mei Hui; Tan, Kevin Bo Lin; Lee, Xi Wen; Oh, Zi Ying; Foo, Fang Jie</i>  AMD, Singapore	B4.1 (P1357) Investigation of UBM/RDL Contact Resistance Based on ICP Sputter Etch Conditions and Critical Design Dimensions  <i>Carazzetti, Patrik (1); Drechsel, Carl (1); Haertl, Nico (1); Weichart, Jürgen (1); Viehweger, Kay (2); Strolz, Ewald (1)</i>  Eveatec AG, Switzerland (1)	B5.1 (P1230) Investigation Of Multi Beam Laser Grooving Process And Die Strength for 55nm Code Low-k Wafer  <i>Xia, Mingyue; Wang, Jianhong; Xu, Sean; Li, guangming; Liu, haiyan; Zhu, lingyan</i>  NXP, China	B6.1 (P1274) Real-time Evaluation of Effective Thermal Conductivity Profile for the Redistribution Layer (RDL)  <i>Liu, Jun; Li, Yangfan; Cao, Shuai; Sridhar, N.</i>  IHPC, A*STAR, Singapore
11:05am - 11:25am	B1.2 (P1316) Parylene as an adhesive for wafer and chip bonding as well as for applications in wafer level packaging  <i>Selbmann, Franz (1,2); Kühn, Martin (1,2); Roscher, Frank (1); Wiemer, Maik (1); Kuhn, Harald (1,3); Joseph, Yvonne (2)</i>  Fraunhofer Institute for Electronic Nano Systems, Germany (1)	B2.2 (P1134) Solder Ball Alloy Effect on Board Level Reliability Thermal Cycling and Vibration Test Enhancement  <i>Chen, Fa-Chuan (1); Yu, Kevin (1); Lin, Shih-Chin (1); Chu, Che-Kuan (2); Lin, Tai-Yin (2); Lin, Chien-Min (2)</i>  Mediatek, Taiwan	B3.2 (P1125) Analysis of Indium-Silver Alloy Thermal Interface Material Reliability and Coverage Degradation Mechanisms  <i>MinJae Kong, DongHyeon Park, Won Ree, YoungJun Koo, JoHyun Bae, YeonKi Jeong, EunSook Sohn, DongSu Ryu, DongJoo Park and KyungRok Park</i>  Amkor, Korea	B4.2 (P1389) Precise Wavelength Control in Fabry-Perot Filters using Thin Etch Stop Layers  <i>Babu Shylaja, Tina; Tack, Klaas; Sabuncuoglu Tezcan, Deniz</i>  IMEC, Belgium	B5.2 (P1215) An Optimization Study with Batch Microwave Plasma On Extra  <i>LOO, Shei Meng; LEONE, Federico; CAICEDO, Nohora</i>  STMicroelectronics, France	B6.2 (P1282) POD-ANN Thermal Modelling Framework for Rapid Thermal Analysis of 2.5D Chiplet Designs  <i>Li, Yangfan; Liu, Jun; Cao, Shuai; Sridhar, Narayanaswamy</i>  IHPC, A*STAR, Singapore
11:25am - 11:45am	B1.3 (P1368) Process Development of Chip to Wafer Hybrid Bonding with Polymer Passivation  <i>Xie, Ling</i>  Institute of Microelectronics, Singapore	B2.3 (P1185) Navigating the Optimal Material Selection for RF Transmission Lines in Cryogenic Systems  <i>Lau, Daniel (1); Bhaskar, Vignesh Shanmugam (1); Ng, Yong Chyn (1); Zhang, Yiyu (2); Goh, Kuan Eng Johnson (2); Li, Hongyu (1)</i>  Institute of Microelectronics, Singapore	B3.3 (P1225) Selection of Non-clean Flux for Metal TIM  <i>Li, Dai-Fei; Teng, Wen-Yu; Hung, Liang-Yih; Kang, Andrew; Wang, Yu-Po</i>  Siliconware Precision Industries Co., Ltd., Taiwan	B4.3 (P1348) Packaging technology for Sub-terahertz antenna in module  <i>Murayama, Kei (1); Taneda, Hiroshi (1); Tsukahara, Makoto (1); Hasaba, Ryosuke (2); Morishita, Yohei (2); Nakabayashi, Yoko (1)</i>  Shinko Electric Industries Co., Ltd, Japan (1); Panasonic, Japan (2)	B5.3 (P1255) In-situ Characterization of Plasma Species for Process Optimization and Improvement  <i>Chou, Djamilia; Capellaro, Laurence; Caicedo, Nohora</i>  STMicroelectronics, France	B6.3 (P1171) Effect of Contact Characteristics on Thermal Contact Resistance of Grease-less Uniform Contact Surfaces  <i>Aoki, Hirotoshi (1); Fushinobu, Kazuyoshi (2); Tomimura, Toshio (3)</i>  KOA Corporation, Japan (1)
11:45am -1:00pm	<b>EPTC Luncheon @ Waterfront Ballroom Level 2</b> <b>(Including the presentation of Best Papers Awards and Publicity by Partner Conferences)</b>					

DAY 3: December 5, 2024 (Thursday PM)

Exhibition at Waterfront Foyer from 9:00am to 5:30pm (Level 2)

Venue	Veranda I	Veranda II	Veranda III	Riverfront I	Riverfront II	Riverfront III
1:00pm - 2:00pm	<b>C1. Electrical Simulations &amp; Characterization 1</b>	<b>C2. Wireless and Antenna Package Designs</b>	<b>C3. Materials and Processing 1</b>	<b>C4. Mechanical Simulation &amp; Characterization 1</b>	<b>C5. TSV and Wafer Level Packaging 2</b>	<b>C6. Thermal Management and Characterization 3</b>
1:00pm - 1:20pm	C1.1 (P1108) Signal integrity analysis of dense wire channels on 2.5D substrate technologies for UCLe and BOW applications <i>Rotaru, Mihai Dragos</i> <i>Institute of Microelectronics, Singapore</i>	C2.1 (P1397) A Compact 1x4 Antenna Array with Steerable Beam for 5G millimeter-Wave Smartphone Applications <i>Hsieh, Sheng-Chi</i> <i>ASE Group, Taiwan</i>	C3.1 (P1159) Photosensitive aqueous alkaline developable magnetic material for inductor and balun transformers in 3D WLP <i>Masuda, Seiya; Idei, Hiroaki; Miyata, Tetsushi; Oi, Shota; Suzuki, Hiroyuki</i> <i>FUJIFILM Corporation, Japan</i>	C4.1 (P1324) Copper balance and wafer level warpage control and effect of package stress and board-level TC solder joint reliability <i>Mandal, Rathin</i> <i>Institute of Microelectronics, Singapore</i>	C5.1 (P1396) Advantages of Digital Lithography in Patterning of UHD FoWLP Utilizing Novel PI Dielectrics <i>Varga, Ksenija</i> <i>EV Group, Austria</i>	C6.1 (P1354) Efficient Thermal-Aware Floor-planning with Bayesian Optimization: A Simulation-Efficient Approach <i>Zhuang, Furen (1); Pratim Kundu, Partha (1); Kircali Sezin, Ata (1); Hou, Yubo (1); Dutta, Rahul (2); James, Ashish (1)</i> <i>Institute for Infocomm Research, Singapore</i>
1:20pm - 1:40pm	C1.2 (P1161) Design of Underground Structure Cover with Self-Complementary Slits for Wireless Telecommunication Application <i>Rong, Zihao (1); Yi, Yuantong (1); Tateishi, Eiichi (2); Kumagae, Takaya (2); Kai, Nobuhiro (2); Yamaguchi, Tatsuya (3); Kanaya, Haruichi (1)</i> <i>Kyushu University, Japan (1)</i>	C2.2 (P1139) Development of 2.4GHz band L-shaped Circular Polarized slot antenna <i>Suehiro, Kazuki; Nakashima, Kenta; Kanaya, Haruichi</i> <i>Kyushu University, Japan</i>	C3.2 (P1118) New DA Adhesive Meets Challenging Performance, Reliability and Cost Objectives of Automotive MCU Packaging <i>Kang, Jaeik; Hong, Xuan; Zhuo, Qizhuo; Yun, Howard; Shim, Kail; Rathnayake, Lahiru; Surendran, Rejoy; Trichur, Ram</i> <i>Henkel, USA</i>	C4.2 (P1340) Material sensitivity of a fan-out package warpage – simulations and experimental validation <i>Tippabhotla, Sasi Kumar; Soon Wee, David Ho</i> <i>Institute of Microelectronics, Singapore</i>	C5.2 (P1193) Chip to Wafer and Wafer to Wafer Density estimation and Design rules physical verification. <i>Mani, Raju; Dutta, Rahul; Cheemalamarri, Hemanth Kumar; Vasarla Nagendra, Sekhar</i> <i>Institute of Microelectronics, Singapore</i>	C6.2 (P1343) Optimizing Chiplet Placement in Thermally Aware Heterogeneous 2.5D Systems Using Reinforcement Learning <i>Kundu, Partha Pratim (1); Furen, Zhuang (1); Sezin, Ata Kircali (1); Yubo, Hou (1); Dutta, Rahul (2); James, Ashish (1)</i> <i>Institute for Infocomm Research, Singapore (1)</i>
1:40pm - 2:00pm	C1.3 (P1167) Equivalent Electromagnetic Radiation Model of Chip Based on Near-Field Scanning for EMI Analysis in Ceramic SiP <i>Liang, Yaya; Du, Pingan</i> <i>UESTC, China</i>	C2.3 (P1203) Development of Long-Range Wireless Energy Harvesting Circuit by Multistage Cockcroft-Walton Circuit <i>Tagawa, Nobuya; Hosaka, Ryoma; Tanaka, Hayato; IGoodwill, Kumar; Kanaya, Haruichi</i> <i>Kyushu University, Japan</i>	C3.3 (P1246) Doped SAC Solder Ball Alloys Comparison for High Performance Automotive BGA Packages <i>Grollier-lee, Stelliane (1); Capellaro, Laurence (1); Mon, Aye aye (2); Wang, Kim-Sing (2); Loh, Hung-Meng (2); Caicedo, Nohora (1)</i> <i>STMicroelectronics (1)</i>	C4.3 (P1147) Advanced Prediction Model for SACQ Solder Reliability Assessment for Automotive Memory Applications <i>Pan, Ling (1); Che, Faxing (1); Ong, Yeow Chon (1); Yu, Wei (1); Ng, Hong wan (1); Kumar, Gokul (2); Fan, Richard (3); Hsu, Pony (3)</i> <i>Micron Semiconductor Asia Operations, Singapore (1)</i>	C5.3 (P1374) Panel Level Fine Patterning RDL Interposer Package <i>Park, Jieun; Kim, Dahee; Choi, Jaeyoung; Park, Woosook; Choi, Yunchan; Lee, Jeongho; Choi, Wonkyoung</i> <i>Samsung Electronics, South Korea</i>	C6.3 (P1259) From Package Thermal Measurements to Material Characterization: A Remote Phosphor Aging Test <i>Hegedüs, János; Takács, Dalma; Hantos, Gusztáv; Poppe, András</i> <i>Budapest University of Technology and Economics</i>
2:00pm - 3:20pm	<b>D1. Electrical Simulations &amp; Characterization 2</b>	<b>D2. Interconnection Technologies 2</b>	<b>D3. Materials and Processing 2</b>	<b>D4. Mechanical Simulation &amp; Characterization 2</b>	<b>Heterogeneous Integration Workshop at Riverfront II and III (2:15pm to 4:15pm)</b>	
2:00pm - 2:20pm	D1.1 (P1272) Crosstalk Analysis for Symmetric and Asymmetric High-Speed Signal Lines of GDDR6 Package <i>Jaiswal, Anushruti (1); Krishna, Vamsi (1); Dhanekula, Mahesh Babu (1); Desmond Dsilva, Hansel (2)</i> <i>Ansys, India (1); Acronix (2)</i>	D2.1 (P1146) Assembly of Multi-Device Power Package with Clips as Interconnects <i>Wai, Leong Ching; Yeo, Yi Xuan; Soh, Jacob Jordan; Tang, Gongyue</i> <i>Institute of Microelectronics, Singapore</i>	D3.1 (P1137) Novel Residue free High Lead Solder Paste for Power discrete <i>Bai, Jinjin; Li, Yanfang; Liu, Xinfang; Chen, Fen; Liu, Yan</i> <i>Indium, China</i>	D4.1 (P1205) Impact of Structural Parameters on the Warpage of fcBGA Packages with Indium TIM <i>Liu, Zhen (1); Dai, Qiaobo (1); Nie, Linjie (1); Xu, Lanying (1); Teng, Xiaodong (1); Zheng, Boyu (1,2)</i> <i>Changsha AnMuQuan Intelligent Technology, China (1)</i>	2:15pm - 2:20pm	Welcome and agenda review: Surya Bhattacharya (IME)
2:20pm - 2:40pm	D1.2 (P1355) Signal Integrity Simulation and Analysis for 2.5D Advanced Package Interconnect Based on UCLe <i>Fan, Yuxuan (1,2); Gan, Hanchen (1,2); Zhou, Yunyan (1); Lei, Bo (1); Song, Gang (1); Wang, Qidong (1)</i> <i>IMECAS, China (1)</i>	D2.2 (P1129) Characterization of Recycled Gold Bonding Wire on Memory Package <i>Chen, Yi-jing; Zou, Yung-Sheng; Chung, Min-Hua; Gan, Chong-Leong</i> <i>Micron, Taiwan</i>	D3.2 (P1220) Low Flux Residue No-Clean Solder Paste for System-in-Package (SiP) Application <i>Liu, Xinfang; Bai, Jinjin; Chen, Fen; Liu, Yan</i> <i>Indium, China</i>	D4.2 (P1141) Impact of Package Warpage on Package Strength Assessment under Three-Point Bending Test Condition <i>Che, Fa Xing (1); Ong, Yeow Chon (1); Yu, Wei (1); Pan, Ling (1); Ng, Hong Wan (1); Kumar, Gokul (2); Takiar, Hem (2)</i> <i>Micron Semiconductor Asia Operations, Singapore (1)</i>	2:20pm - 2:30pm	Opening Remarks (Jeff Suhling, Auburn Univ., IEEE President Elect)
2:40pm - 3:00pm	D1.3 (P1223) Effect of Mesh Ground Plane on Impedance Control and Crosstalk of Organic Interposers Targeted for Chiplet Applications <i>Lim, Ying Ying (1); Nemoto, Shunsuke (2)</i> <i>National Institute of Advanced Industrial Science and Technology, Japan (1)</i>	D2.3 (P1126) Investigation of the Electromigration Behaviour of Solder Bump under Different Conditions <i>Law, Yi Kei Owen (1); Fan, Haibo (1); Zhong, Chenchao Nick (1); Shi, Yuning (2)</i> <i>Nexperia, Hong Kong</i>	D3.3 (P1176) Analysis of Basic Properties and Bonding Properties of Various Melting Temperature Solders <i>Kim, Hui Joong; Lee, Jace; Lee, Seul Gi; Son, Jae Yeol; Won, Jong Min; Park, Ji Won; Kim, Byung Woo; Shin, Jong Jin; Lee, Tae Kyu</i> <i>MKE, South Korea</i>	D4.3 (P1181) Evaluation of Thermo-mechanical Fatigue life of Microvias under PCB Substrate's influence during Reflow Process <i>Syed, Mujahid Abbas; Yu, Qiang</i> <i>Yokohama National University, Japan</i>	2:30pm - 2:40pm	Impact of Chiplets on Packaging Architecture (Subu Iyer, UCLA)
3:00pm - 3:20pm	D1.4 (P1241) Development of Compact Wideband Balun using Multilayer Substrate-integrated Coaxial line <i>Sato, Takumi (1); Kanaya, Haruichi (1); Ichirizuka, Takashi (2); Yamada, Shusaku (2)</i> <i>Kyushu University, Japan (1)</i>	D2.4 (P1168) Investigation of NiSn4 formation in the Relation between SnBi Solder and ENEPIG Substrate <i>Wang, Yi-Wun; Tsai, Cheng-Ting; Lin, Tzu-Yi</i> <i>Tamkang University, Taiwan</i>	D3.4 (P1124) A Novel Method for PBO Adhesion Characterization in WLCSF Package <i>CHEN, Yong; CHANG, Jason; GANI, David; LUAN, Jing-en; CATTARINUZZI, Emanuele</i> <i>STMicroelectronics, Singapore</i>	D4.4 (P1160) Improved Thermal performance of 3D Opto-Electronic IC assembled on multiple Interposers through design optimization <i>Rekapalli, Vamsi (2); Mohammed, Ubed (2); V Ramana, Pamidighantam (1); Yeluripati, Rohin Kumar (1); Bhandari, Jugal Kishore (2); Dharavath, Sandhya (2)</i> <i>Lightspeed Photonics, Singapore</i>	2:40pm - 3:00pm	Interconnect Technologies for Heterogeneous Integration (Vempati Srinivasa Rao, IME)
3:20pm - 4:20pm	Interactive Poster Presentation II / Exhibition / Coffee Break @ Waterfront foyer (Level 2)					
4:20pm - 6:05pm	Exhibitor Presentations at Riverfront I, II and III – Plus Quiz & Prizes!					
6:05pm - 7:30pm	Sponsors & Exhibitors Cocktail & Networking Session @ Lyrebird Level 3 (by invitation only)					
3:00pm - 3:20pm					3:00pm - 3:10pm	Equipment Process Innovation for Advanced Packaging (Loke Yuen Wong, AMAT)
					3:10pm - 3:20pm	Materials Innovations for Heterogeneous Integration (Kaz Yamamoto, Hitachi Chemicals)
					3:20pm - 3:35pm	SHINE: Innovating for HI Infections (Aaron Thean, NUS)
					3:45pm - 4:15pm	Panel Discussion: Subu Iyer (UCLA), Gamal Refai Ahmed (AMD), Patrick Lo, (AMF), Carlos Mazure, (IME), Aaron Thean (NUS), Yu Po Wang (SPIL)

DAY 4: December 6, 2024 (Friday)						
Exhibition at Waterfront Foyer from 9:00am to 4:30pm (Level 2)						
Venue	Waterfront I	Waterfront II	Waterfront III	Riverfront I	Riverfront II	Riverfront III
09:00am -10:20am	<b>E1. Assembly and Manufacturing Technology 2</b>	<b>E2. Emerging Technologies 2</b>	<b>E3. Materials and Processing 3</b>	<b>E4. Mechanical Simulation &amp; Characterization 3</b>	<b>E5. Quality, Reliability &amp; Failure Analysis 1</b>	<b>E6. Silicon Interposer and Processing</b>
09:00am - 9:20am	E1.1 (P1175) Investigation on Molding Void Issue in System-in-Package Module <i>Yang, Chaoran; Tang, Oscar; Song, Fubin</i> <i>Amazon, China</i>	E2.1 (P1352) CMOS compatible 2D material integration for Sensor Applications on 200mm wafers <i>Yoo, Tae Jin; Tezcan, Deniz Sabuncuoglu</i> <i>IMEC, Belgium</i>	E3.1 (P1247) Study on Microstructure and Mechanical Properties of Silver and Silver-Indium Solid Solution Films Using Magnetron Sputtering <i>Zhao, Shuang (1); Lin, Pengrong (2,3); Zhang, Donglin (1); Wang, Taiyu (1); Liu, Sichen (1); Xie, Xiaochen (2); Xu, Shimeng (2); Qu, Zhibo (2); Wang, Yong (2); Zhao, Xiuchen (1); Huo, Yongjun (1,4)</i> <i>Beijing Institute of Technology, China (1)</i>	E4.1 (P1121) Analytical K-factor Model for Monotonic Four-point Bend Test Design <i>Kelly, Brian (1); Tarnovetchi, Marius (2); Newman, Keith (1)</i> <i>AMD, USA (1); Vitecos, Romania (2)</i>	E5.1 (P1164) Non-Destructive Analysis of Voiding in TIM of High-Performance Computing Devices using B-mode Scanning <i>Song, Mei Hui; Tang, Wai Kit; Tan, Li Yi</i> <i>AMD, Singapore</i>	E6.1 (P1207) Adaptive Pad Stacks Deliver Order of Magnitude Increase in Bridge Die Position Tolerance in Embedded Fan-out Interposers <i>Sandstrom, Clifford Paul (1); Talain, John Erickson Apellido (1); San Jose, Benedict Arcena (1); Fang, Jen-Kuang (2); Yang, Ping-Feng (2); Huang, Sheng-Feng (2); Shen, Ping-Ching (2)</i> <i>Deca Technologies, USA (1); ASE Global (2)</i>
9:20am - 9:40am	E1.2 (P1172) Enhancing DI Water Cleanability of Tacky Flux on Cu OSP Surface Using FC Copper Pillar High-Density Interconnection <i>Lip Hueli, Yam; Risson Olakkankal, Edrina; Balasubramanian, Senthil Kumar</i> <i>Heraeus Materials Singapore</i>	E2.2 (P1384) Hyperspectral Component Fabrication on 200mm CMOS Image Sensor Wafer <i>Babu Shylaja, Tina; Yoo, Tae Jin; Geelen, Bert; Tack, Klaas; Sabuncuoglu Tezcan, Deniz</i> <i>IMEC, Belgium</i>	E3.2 (P1206) Versatile Photosensitive Polymer Applied in Low-Temperature Hybrid Bonding with Nanocrystalline Cu <i>Tan, Chung-An (1); Lee, Chia-Hsin (1); Lee, Ou-Hsiang (2); Chiu, Wei-Lan (2); Chang, Hsiang-Hung (2); Yu, Shih-cheng (2)</i> <i>Brewer Science, Taiwan (1); ITRI Taiwan (2)</i>	E4.2 (P1135) Enhancing Mechanical Robustness and Integrity of a Large Advanced Package with Embedded FP Interconnect Chips <i>Ji, Lin; Chai, Tai Chong</i> <i>STMicroelectronics, Singapore</i>	E5.2 (P1361) A Method for Die-level Fracture Toughness Evaluation by Nano-Indentation on Ring <i>Zhu, Xintong; Rajoo, Ranjan; Nistala, Ramesh Rao; Mo, Zhi Qiang</i> <i>Globalfoundries, Singapore</i>	E6.2 (P1119) Silicon Interposer Heterogeneous Integration Platform for Millimeter Wave Ka and V band Satellite Applications <i>Sun, Mei; Ong, Javier Jun Wei; Wu, Jia Qi; Lim, Sharon Pei Siang; Ye, Yong Liang; Umraikar, Ratan Bhimrao; Lau, Boon Long; Lim, Teck Guan; Chai, Kevin Tshun Chuan</i> <i>Institute of Microelectronics, Singapore</i>
9:40am - 10:00am	E1.3 (P1326) Film Assisted Molding Performance Improvement with Component Design <i>Law, Hong Cheng; Lim, Ful Yee; Low, Boon Yew; Pang, Zi Jian; Bharatham, Logendran; Yusof, Azaharudin; Ismail, Rima Syafida; Lim, Denyse Shyn Yee; Lim, Shea Hui</i> <i>NXP, Malaysia</i>	E2.3 (P1390) Characterization of Carbon Contained Films at Bonding Interface for the Application of Backside Power Delivery Networks <i>Kitagawa, Hayato; Sato, Ryoosuke; Fuse, Junrya; Yoshihara, Yuki; Inoue, Fumihito</i> <i>Yokohama National University, Japan</i>	E3.3 (P1286) Low temperature Ag sintering and driving force on Au finished Cu substrates at 145°C and 175°C using Ag nano-porous sheets without organic solvents <i>Kim, YehRi (1,2); Yu, Haiyoung (1); Noh, Seungjun (3); Kim, Dongjin (1)</i> <i>Korea Institute of Industrial Technology (1)</i>	E4.3 (P1116) Study on Substrate Copper Pad Crack Through Experiment and Simulation <i>Yu, Wei; Che, Fa Xing; Ong, Yeow Chon; Pan, Ling; Cheong, Wee Gee</i> <i>Micron Semiconductor Asia Operations, Singapore</i>	E5.3 (P1140) Electrostatically induced voltage generated in different type boxes of electronic equipment by moving charged object <i>Ichikawa, Norimitsu</i> <i>Kogakuin University, Japan</i>	E6.3 (P1138) Development of Large RDL Interposer Package: RDL-first FOWLP and 2.5D FO-Interposer <i>Ho, Soon Wee David; Soh, Siew Boon; Lau, Boon Long; Hsiao, Hsiang-Yao; Lim, Pei Siang; Rao, Vempati Srinivasa</i> <i>Institute of Microelectronics, Singapore</i>
10:00am - 10:20am	E1.4 (P1224) An Investigation of Different Leadframe Materials with Plasma Cleaning on Extra-Large Leadframe to Study the Effects of Oxidation vs Delamination <i>CHUA, Yeechong; CHUA, Boowei; LEONE, Federico; LOO, Shei Meng</i> <i>STMicroelectronics, Singapore</i>	E2.4 (P1376) Screen Printed Temperature Sensor using Novel Kish Graphite/reduced Graphene Oxide Conductive Ink for Wearable Applications <i>Rao, Ankitha (1); Bhat, Somashankara (1); De, Shounak (1); Shetty K, Nakul (1); Nayak, Ramakrishna (2)</i> <i>Manipal Institute of Technology, India (1)</i>	E3.4 (P1179) Exploring Direct Laser Reflow Techniques for Forming Stable and Reliable Solder Bump Interfaces on Semiconductor Substrates <i>Fettke, Matthias; Fisch, Anne; Teutsch, Thorsten</i> <i>PacTech, Germany</i>	E4.4 (P1130) Predictive Numerical Modeling of Stealth Dicing Process for Different Wafer Pre-Thin Thicknesses <i>Lim, Dao Kun (1,2); Vempaty, Venkata Rama Satya Pradeep (2); Shah, Ankur Harish (2); Sim, Wen How (2); Singh, Harjashan Veer (2); Lim, Yeow Kheng (1)</i> <i>Micron Technology, Singapore (1); NUS Singapore (2)</i>	E5.4 (P1350) High spatial resolution imaging of dopants and impurities for semiconductor device using NanoSIMS <i>Sameshima, Junichiro; Nakata, Yoshihiko; Akahori, Seishi; Hashimoto, Hideki; Yoshikawa, Masanobu</i> <i>Toray Research Center, Inc, Japan</i>	E6.4 (P1209) Modeling and Fabrication of Silicon Integrated Multi-terminal Deep Trench Capacitor Technology <i>Lin, Weida (1); Song, Changming (2); Shao, Ziyuan (3); Ma, Haiyan (2); Cai, Jian (2,4); Gao, Yuan (1); Wang, Qian (2,4)</i> <i>Tsinghua University, China (1)</i>
10:20am - 10:35am	Tea Break & Exhibition (Waterfront Ballroom Foyer)					
10:35am -11:55am	<b>F1. Automotive and Power Device Packages</b>	<b>F2. Quality, Reliability &amp; Failure Analysis 2</b>	<b>F3. Materials and Processing 4</b>	<b>F4. Advacned Optoelectronics</b>	<b>F5. Electrical Simulations &amp; Characterization 3</b>	<b>F6. Thermal Management and Characterization 4</b>
10:35am -10:55am	F1.1 (P1234) A Highly Integrated AIP Design for 6G Application <i>WU, PO-I; Kuo, Hung-Chun; Jhong, Ming-Fong; Wang, Chen-Chao</i> <i>ASE Group, Taiwan</i>	F2.1 (P1184) Optimization of Aluminium Wirebonding on Niobium for Cryogenic Packaging <i>Norhanani Jaafar</i> <i>Institute of Microelectronics, Singapore</i>	F3.1 (P1254) Study of Interactions between RDL Polyimides and Underfills on Reliability of Flip-Chip Interconnects in Thermal Cycling <i>Chang, Hongda (1); Soriano, Catherine (1); Chen, WenHsuan (1); Yang, HungChun (2); Lai, WeiHong (2); Chaware, Raghunandan (1)</i> <i>Lattice Semiconductor Corp, Taiwan; ASE Global (2)</i>	F4.1 (P1252) Aerosol Jet Printed Encapsulation for Optoelectronics: A Study of Line Morphology <i>Siah, Kok Siong (1); Basu, Robin (2); Distler, Andreas (2); Häudler, Felix (1); Franke, Jörg (1); Bräbe, Christoph J. (2,3,4); Egelhaaf, Hans-Joachim (2,3,4)</i> <i>Friedrich-Alexander Universität Erlangen Nürnberg, Germany (1)</i>	F5.1 (P1201) Effect of Decoupling Capacitor Location on PDN Impedance in fBGAs Packages <i>Song, Xiaoyuan (1); Zheng, Boyu (1,2); Luo, Jiahui (1); Wei, Ping (1); Liu, Lei (1)</i> <i>Changsha Anmuquan, China (1)</i>	F6.1 (P1258) Thermal Characterization of LED Packages Covered with Wavelength Converting Phosphor Over a Large Area <i>Hantos, Gusztáv; Hegedüs, János; Lipák, Gyula; Németh, Márton;Poppe, András</i> <i>Budapest University of Technology and Economics</i>
10:55am - 11:15am	F1.2 (P1298) Packaging-Codesign for the development of a high-resolution MIMO-Radar-Module for Automated guided vehicles <i>Tschoban, Christian; Pötter, Harald</i> <i>Fraunhofer IZM, Germany</i>	F2.2 (P1182) In-Situ Microcrack Localization and Imaging in Laminated Die-Attachment Based on the Static Component of Ultrasonic Lamb Waves <i>Long, Xu (1); Li, Yaxi (2); Wang, Jishuo (3); Zhao, Liang (3); Yuan, Weifeng (3)</i> <i>Northwestern Polytechnical University, China</i>	F3.1 (P1179)An Innovative Flux-Less Solder Ball Attachment Technology (FLAT) for Advanced BGA Assembly <i>Kim, Dongjin (1); Han, Seonghui (1,3); Han, Sang Eun (1,4); Choi, Dong-Gyu (1,5); Chung, Kwansik (2); Kim, Eunhae (2); Yoo, Sehoon (1)</i> <i>Korea Institute of Industrial Technology (1)</i>	F4.2 (P1341) Quantum Cascade Laser Integration with Mid-Infrared Photonic Integrated Circuits for Diverse Sensing Applications <i>Kannojia, Harindra Kumar (1); Zhai, Tingting (1); Maulini, Richard (2); Gachet, David (2); Kuyken, Bart (1); Van Steenberge, Geert (1)</i> <i>IMEC, Belgium (1)</i>	F5.2 (P1200) A Novel Approach to Reduce Impedance Discontinuities for High-speed Channel in IC Packages <i>Luo, Jiahui (1); zheng, Boyu (1,2); Song, Xiaoyuan (1); Jiang, Bo (1); Lee, SooLim (1)</i> <i>Changsha Anmuquan, China</i>	F6.2 (P1289) Numerical Optimization of PCM-Based Heat Sink for Thermal Management of High-power-density Electronics <i>HU, RAN (1,2); Du, Jianyu (2); Shi, Shangyang (1,2); Lv, Peijue (1,2); Cao, Huiquan (2); Jin, Yufeng (1,2); Zhang, Chi (2,3,4); Wang, Wei (2,3,4)</i> <i>Peking University, China</i>
11:15am - 11:35am	F1.3 (P1306) Robustness Methodology for Next Generation Automotive Microcontroller Flip Chip Copper Pillar Technologies <i>Tan, Aik Chong; Bauer, Robert; Rau, Ingolf; Doering, Inga</i> <i>Infinion Technologies, Singapore</i>	F2.3 (P1122) BLR Drop Test Study for FCCSP Package with OSP/Cu Solder Pad finish <i>Liu, Jimmei</i> <i>NXP Semiconductor Company, China</i>	F3.3 (P1281) Elimination of Parametric Shifts in Trench MOSFETs Using Low Alpha-Particle Solder <i>Gajda, Mark A. (1); de Leon, Charles Daniel T. (2); A/P Ramalingam, Vegneswary (3); Santican, Haima (3)</i> <i>Nexperia, United Kingdom</i>	F4.3 (P1328) III-V Laser Diode Flip Chip Bonding on Photonics Integrated Circuit with SnAg Solder <i>Chi, Ting Ta (1); Ser Choong, Chong (1); Lee, Wen (1); Yuan, Xiaojun (2)</i> <i>Institute of Microelectronics, Singapore (1); LIINKSTAR (2)</i>	F5.3 (P1304) Full-Wave Electromagnetic Simulation Approach for Integrated 3D-IC Design <i>Jaiswal, Anushruti; Patil, Tejikiran; Dhankula, Mahesh Babu</i> <i>Ansys, India</i>	F6.3 (P1288) Heat-Resistant Reliability of Large Area Silver Micro porous Connections for Direct Cooling in Power Inverter Applications <i>Yu, HaYoung; Kim, Seoh; Kim, Dongjin</i> <i>Korea Institute of Industrial Technology</i>
11:35am - 11:55pm	F1.4 (P1387) Bond Strength Comparison of Commercial and Custom Copper Sinter Pastes under Sinter Process Modifications <i>Meyer, Meyer; Gierth, Karl Felix Wendelin;Meier, Karsten; Bock, Kartheinz</i> <i>Technische Universität Dresden, Germany</i>	F2.4 (P1236) Influence of Material Composition on Copper-aluminum Wire Bonding Reliability <i>Carluccio, Roberta (1); Caglio, Carolina (1); Alesi, Mirko (1); Mancaloni, Alberto (1); Villa, Riccardo (1); Serafini, Andrea (1); Dellasega, David (2)</i> <i>STMicroelectronics, Italy (1)</i>	F3.4 (P1218) Effects of Bi contents in Sn-SAg lead-free solders on mechanical properties and morphology of IMC <i>Liu, Kuan Cheng; Li, Chuan Shun; Teng, Wen Yu; Hung, Liang Yih; Wang, Yu Po</i> <i>Siliconware Precision Industries Co., Ltd., Taiwan</i>	F4.4 (P1128) Generation of Beam Profiles from Chip-to-Free-Space Coupling using Deep Neural Network <i>Lim, Yu Dian (1); Tan, Chuan Seng (1,2)</i> <i>Nanyang Technological University, Singapore (1)</i>	F5.4 (P1162) Discussion on the Electrical Characteristics of Tera-Hz in Organic Substrate <i>Lin, Ho-Chuan; Lai, Chia-Chu; Shih, Teny; Kang, Andrew; Wang, Yu-Po</i> <i>Siliconware Precision Industries Co., Ltd., Taiwan</i>	F6.4 (P1199) A Study on Thermal Performance Enhancement for Multi-chip Power μModules <i>Dai, Qiaobo (1); Liu, Zhen (1); Liao, Jinjie (2); Zheng, Boyu (1,3); Liu, Zheng (1); Yuan, Sheng (1)</i> <i>Changsha Anmuquan, China (1)</i>
11:55am - 12:55pm	Lunch @ Waferfront Foyer (Level 2)					

DAY 4: Decemr 6, 2024 (Friday PM)  
Exhibition at Waterfront Foyer from 9:00am to 4:30pm (Level 2)

Venue	Waterfront I	Waterfront II	Waterfront III	Riverfront I	Riverfront II	Riverfront III
12:55pm - 2:15pm	<b>G1. Bonding &amp; Debonding Processes</b>	<b>G2. Wafer Processing and Characterization 2</b>	<b>G3. Materials and Processing 5</b>	<b>G4. Smart Manufacturing, Equipment &amp; Tooling Co-Design</b>	<b>G5. TSV and Wafer Level Packaging 3</b>	<b>G6. Embedded and Fan-Out Packaging</b>
12:55pm - 01:15pm	G1.1 (P1380) High-temp-stable temporary bond adhesive for IR laser debonding enables new process integration for thin wafers <i>Koch, Matthew (1); Kumar, Amit (1); Brandt, Elisabeth (2); Bravin, Julian (2); Urban, Peter (2); Geier, Roman (3); Segert, Joerg (3)</i> Brewer Science, United Kingdom (1)	G2.1 (P1411) Patterning of 1µm Critical Dimension Through Silicon Via using Positive Tone Resist Mask by a Photolithography Stepper <i>Sundaram, Arvind (1); Kang, Riley (2); Bhesetti, Chandra Rao (1)</i> Institute of Microelectronics, Singapore (1)	G3.1 (P1198) Influence of Flow Rate and Current Density on Copper Deposition in Through Hole <i>Zeng, Barry; Ye, Rick; Pai, Yu-Cheng; Wang, Yu-Po</i> Siliconware Precision Industries Co., Ltd., Taiwan	G4.1 (P1309) Exploring Diffusion Model for Semiconductor Defect Detection <i>Lu, Kangkang; Cai, Lile; XU, Xun; Pahwa, Ramanpreet; Wang, Jie; Chang, Richard; Foo, Chuan-Sheng</i> Institute for Infocomm Research, Singapore	G5.1 (P1180) Optimization of High Aspect Ratio Copper Pillar Fabrication for Through Mold Interposer (TMI) Processing <i>Peh, Cun Jue; Lau, Boon Long; Chia, Lai Yee; Ho, Soon Wee.</i> Institute of Microelectronics, Singapore	G6.1 (P1202) Integration Module of Dual MOSFET Switching Circuit Using Embedded Silicon Fan-Out (eSiFO®) Technology <i>Qiang, Wenbin; Zhang, Xiangou; Sun, Xiangyu; Deng, Shualrong; Yang, Zhenzhong</i> Microsystem and Terahertz Research Center, China
01:15pm - 01:35pm	G1.2 (P1250) Delamination of Temporary Bonded Wafers: A Comprehensive Study <i>Jedidi, Nader</i> IMEC, Belgium	G2.2 (P1410) Niobium - last Process for Multi-foundry-compatible Wafer Level Processing of Superconducting Interposers <i>Goh, Simon Chun Kiat; Ng, Yong Chyn; Ong, Javier Jun Wei; Lau, Daniel; Tseng, Ya-Ching; Jaafar, Norhanani; Yoo, Jae Ok; Liu, Liyuan; Teo, Everline Shu Yun; Chua, Nicholas Boon Leong; Li, Hongyu</i> Institute of Microelectronics, Singapore	G3.2 (P1156) Routable Wettable Flanks for MEMS devices <i>Shaw, Mark; Gritti, Alex; Ratti, Andrea; Wong, Kim-Sing; Loh, Hung-meng; Casati, Alessandra; Antlano Jr, Ernesto; Soreda, Alvin</i> STMicroelectronics, Italy	G4.2 (P1287) End-to-end Fast Segmentation Framework for 3D Visual Inspection of HBMs <i>Wang, Jie (1); Chang, Richard (1); Lim, Meng Keong (2); Chong, Ser Choong (2); Yang, Xulei (1); Pahwa, Ramanpreet Singh (1)</i> Institute for Infocomm Research, Singapore (1)	G5.2 (P1405) Splitting Process Integration for 2.5D/3D Packaging <i>Li, Hongyu (1); Vasarla Nagendra, Sekhar (1); Schwarzenbach, Walter (2); Besnard, Guillaume (2); Lim, Sharon (1); BEN MOHAMED, Nadia (2); Nguyen, Bich-Yen (2)</i> Institute of Microelectronics, Singapore	G6.2 (P1268) Corrosion behavior of aluminium pads in Fan-Out Panel Level Packaging (FOPLP) <i>Yu, Yeonseop; Park, Seyoon; Kim, Myoung; Moon, Taeho</i> Samsung Electronics, South Korea
01:35pm - 01:55pm	G1.3 (P1192) Surface Quality Challenges Associated with Temp Bonding and Debonding for Chip Stacking Applications <i>Chaki Roy, Sangita; Vasarla, Nagendra Sekhar; Venkataraman, Nandini</i> Institute of Microelectronics, Singapore	G2.3 (P1331) A New D2W Bonding Alignment Scheme using Magnetic and Capillary assisted Self-alignment <i>Choi, Daesan (1); Kim, Sumin (2); Hahn, Seung Ho (1); Moon, Bumki (1); Rhee, Daniel Minwoo (1)</i> Samsung Electronics, South Korea	G3.3 (P1183) Understanding and Improving R <sub>c</sub> Management for Wafer Level Packaging through Novel PVD Processing <i>Barker, Anthony James; Haymore, Scott; Wilby, Tony; Rastogi, Amit; Moncrieff, Ian; Jones, Steve; Joanne Chuan Sun</i> KLA-Tencor, United Kindom	G4.3 (P1375) Ultra-thin ta-C Hermetic Seals for Electronics Packaging <i>Phua, Eric Jian Rong; Lim, Song Kiat Jacob; Tan, Yik Kai; Shi, Xu</i> Nanofilm Technologies, Singapore	G5.3 (P1285) Fabrication of Through Alumina Vias: A Cost-effective Alternative Approach Using Ultrasonic Machining and Electroless Deposition <i>Pawar, Karan; Pandey, Harsh; Dixit, Pradeep</i> Indian Institute of Technology Bombay	G6.3 (P1123) Comparison of Electrical, Thermal, and Mechanical Performances of a fcBGA with that of a Fan-Out SiPlet Package <i>Ouyang, Eric; Ahn, Billy; Han, Bi; Han, Michael; Kang, Chen; Oh, Michael</i> Silicon Box
01:55pm - 02:15pm	P1142. Investigating overlay control towards 2.5/3D system integration in backend lithography processes <i>Huang, Chia-Ching (1); Lee, Yutai (1); Lee, Yuan-Chang (2); van der Kraken, Pieter (1); Chang, Liang-Chuan (2); de Boel, Jeroen (1); MISAT, Sylvain Irene (1); Chang, Hsiang-Hung (2); van der Stam, Michel (1)</i> Onto Innovation, Taiwan (1)	G2.4 (P1233) Novel Wet-Chemical Processing for Sidewall Plating of High Reliability Bottom-Terminated Packages <i>Hovestad, Arjan (1); Basu, Tarun (2)</i> Besi, The Netherland	G3.4 (P1240) Dielectric Breakdown of in-Package Epoxy Mold Compound under Wet and Dry Conditions: Frequency and Temperature dependence <i>Balestra, Luigi (1); Riaz, Muhammad Tanveer (1); Giuliano, Federico (1); Cavallini, Andrea (1); Raggiari, Susanna (1); Oldani, Luca (2); Guarnara, Simone Salvatore (2); Rossetti, Mattia (2); Depetro, Riccardo (2)</i> University of Bologna, Italy (1), STMicroelectronics (2)	G4.4 (P1251) Semiconductor MEMS Waferbond Defect Detection: The Industrial Application of ResNets <i>Stoll, Fiete; Dubey, Vikas; Wunsch, Dirk; Roscher, Frank; Wiemer, Malk</i> ENAS Fraunhofer, Germany	G5.4 (P1109) Electrical Characterization and Reliability Studies of TSI with 5-layer Frontside Cu and 2-layer Backside Cu RDL <i>Tseng, Ya-Ching; Lau, Daniel; Ming, Calvin Chua Hung; Li, Hongyu</i> Institute of Microelectronics, Singapore	G6.4 (P1228) Fan-Out Packaging without Warpage <i>Schindler, Markus; Ringelstetter, Severin; Bues, Martin; Kroul, Kilian; Chian, Lim See; Königler, Tobias</i> Delo, Germany
2:15pm - 3:15pm		<b>H2. Quality, Reliability &amp; Failure Analysis 3</b>	<b>H3. Materials and Processing 6</b>	<b>H4. Mechanical Simulation &amp; Characterization 4</b>	<b>H5 Advanced Chip and Package Designs</b>	<b>H6. Flip Chip and Fan-Out on Substrate</b>
2:15pm - 2:35pm		H2.1 (P1362) Lifetime Modelling Strategy for Multilayer Ceramic Capacitors by HALT test <i>Yang, Yongbo; Yong, Eric; Qiu, Wen</i> AMD, Singapore	H3.1 (P1279) Stress compensation effect in AlN/Mo/AlN/Polysilicon stack for MEMS application <i>Sharma, Jaibir; Qing Xin, Zhang</i> Institute of Microelectronics, Singapore	H4.1 (P1197) Dynamic Response of Interconnects in Board-level Packaging Structure at Extremely High Strain Rates <i>Long, Xu (1); Hu, Yuntao (2); Shi, Hongbin (3); Su, Yutai (2)</i> Northwestern Polytechnical University, China (1)	H5.1 (P1320) Process Development of Twin 2 Die Stack Modules for Deep Learning Hardware Accelerator <i>Ser Choong Chong</i> Institute of Microelectronics, Singapore	H6.1 (P1235) Fine-line RDL Structure Analysis of Fan-Out Chip-on-Substrate Platform <i>Lai, Chung-Hung</i> ASE Group, Taiwan
2:35pm - 2:55pm		H2.2 (P1257) Innovative Cu-Selective Passivation Coatings for Enhanced Reliability in Cu Interconnects for IC Packaging <i>Antony Jesu Durai, Kevin (1); Kumaravel, Dinesh Kumar (1); Muralidharan Nair, Shyam (1); Tran, Khanh (1); Chyan, Oliver (1); Poliah, Ramarao (2); Zhi Chan, Mei (3); Mathew, Varughese (4)</i> Univerity of North Texas, USA (1)	H3.2 (P1154) Die Attach Material Choice for MEMS Cavity Packages <i>Shaw, Mark; Simoncini, Daniele; Duca, Roseanne; Falorini, Luca; Carulli, Paola; Fedeli, Patrick; Brignoli, Davide</i> STMicroelectronics, Italy	H4.2 (P1242) Determination of the Adhesive Strength of Monocrystalline Layers as a Thin Film on a Silicon Substrate by Means of Instrumented Indentation Testing <i>Albrecht, Jan; Rzepka, Sven</i> ENAS Fraunhofer, Germany (1)	H5.2 (P1398) Thermal Test Vehicles for Characterization of Thermal Performance of AI Chips <i>Shangguan, Dongkai (1); Yang, Cheng (2); Hang, Yin (3)</i> Thermal Engineering Associates (1), JCET Group (2)	H6.2 (P1131) The FOSTrip® technique - a low-cost solution for the strip level fan-out on substrate package <i>Lin, I-Hung (1); Shih, Meng-Kai (2); Ding, Bo-Rui (2); Lou, Bai-Yao (1); Ni, Tom (1)</i> Kore Semiconductor Co., Ltd., Taiwan (1); National Sun Yat-sen University (2)
2:55pm - 3:15pm		H2.3 (P1370) Embedded Defect Depth Estimation using NIR Model-less TSDM <i>Lee, Jun Ho (1); Joo, Ji Yong (1); Lee, Jun Sung (1); Kim, Se Jeong (1); Kwon, Oh-Hyung (2)</i> Kongju National University, South Korea	H3.3 (P1173) Enhancing Device Performance through Non-Pressure Sintering on Copper Lead frames <i>Danila, Bayaras; Abito; Balasubramanian, Senthil Kumar</i> Heraeus Materials Singapore	H4.3 (P1407) Electromigration Study of Cu Pillar Bumps Using Experimental and Numerical Methods <i>Zhao, Facheng; Zhu, Liping; Yeo, Alfred</i> STATS ChipPAC Singapore	H5.3 (P1261) Cost-Performance Co-Optimization for the Chiplet Era <i>Graening, Alexander Phillip (1); Patel, Darayus Adil (2); Sisto, Giuliano (2); Lenormand, Erwan (2); Perumkunnil, Manu (2); Pantano, Nicolas (2); Kumar, Vinay B.Y. (2); Gupta, Puneet (1); Malik, Arindam (2)</i> UCLA, USA (1)	H6.3 (P1327) Semiconductor Chip and Package Co-Design and Assembly for Dual Use in FC and WB BGA <i>Rongrong Jiang; Trent Uehling, Bihua He; Tingdong Zhou; Meiliang Song; Azham Mohdsukemi; Taki Fang, Roy Lo; Kaelin Wang</i> NXP Semiconductor Company, China
3:15pm - 4:15pm	Interactive Poster Presentation III / Exhibitions / Coffee Break @ Waterfront foyer (Level 2)					
4:15pm - 5:00pm	Closing Ceremony @ Riverfront Ballroom Foyer (Level 2)					
Complete our online survey for a chance to enter our exciting lucky draw! Many fantastic prizes are up for grabs, including the grand prize of an iPhone 16 Plus!						

# Session Chair for Oral Presentation by Day and Track

Date	Time Start	Time End	Tracks	Room	Session Chair
12/05/2024	09:00 AM	10:30 AM	A1. Hybrid and Fusion Bonding 1	Veranda I	Dr Yong-Fen Hsieh, MA-Tek
12/05/2024	09:00 AM	10:30 AM	A2. Wafer Processing and Characterization	Veranda II	Dr Suresh Singaram, Evactec
12/05/2024	09:00 AM	10:30 AM	A3. Emerging Technologies	Veranda III	Prof Kanaya Haruichi, Kyushu University
12/05/2024	09:00 AM	10:30 AM	A4. Advanced Packaging 1	RiverFront I	Dr Wang Yu-Po, Siliconware Precision Industries Co., Ltd
12/05/2024	09:00 AM	10:30 AM	A5. TSV & Wafer Level Packaging 1	RiverFront II	Albert Lan, Applied Materials
12/05/2024	09:00 AM	10:30 AM	A6. Thermal Management and Characterization 1	RiverFront III	Prof Fushinobu Kazuyoshi, Tokyo Institute of Technology
12/05/2024	10:45 AM	11:45 AM	B1. Hybrid and Fusion Bonding 2	Veranda I	Dr James Papanu, Tokyo Electron Limited
12/05/2024	10:45 AM	11:45 AM	B2. Interconnection Technologies 1	Veranda II	Dr Yang Cheng, JCET
12/05/2024	10:45 AM	11:45 AM	B3. Thermal Interface Materials	Veranda III	Senthil Kumar, Heraeus
12/05/2024	10:45 AM	11:45 AM	B4. Advanced Packaging 2	RiverFront I	Dr Torseten Wipiejewski, Huawei
12/05/2024	10:45 AM	11:45 AM	B5. Assembly and Manufacturing Technology 1	RiverFront II	Jing-En Luan, STMicroelectronics Singapore
12/05/2024	10:45 AM	11:45 AM	B6. Thermal Management and Characterization 2	RiverFront III	Hardik Kabaria, Vinci4D
12/05/2024	1:00 PM	2:00 PM	C1. Electrical Simulations & Characterization 1	Veranda I	Prof Masahiro Aoyagi, Kumamoto University
12/05/2024	1:00 PM	2:00 PM	C2. Wireless and Antenna Package Designs	Veranda II	Chia Chu Lai, Siliconware Precision Industries Co., Ltd
12/05/2024	1:00 PM	2:00 PM	C3. Materials and Processing 1	Veranda III	Takenori Fujiwara, Toray
12/05/2024	1:00 PM	2:00 PM	C4. Mechanical Simulation & Characterization 1	RiverFront I	Dr Che Faxing, Micron
12/05/2024	1:00 PM	2:00 PM	C5. TSV and Wafer Level Packaging 2	RiverFront II	Chew Soon Aik, imec
12/05/2024	1:00 PM	2:00 PM	C6. Thermal Management and Characterization 3	RiverFront III	Dr Winston Zhang, Novark Technologies
12/05/2024	3:00 PM	4:20 PM	D1. Electrical Simulations & Characterization 2	Veranda I	Mihai Dragos Rotaru, IME Singapore
12/05/2024	3:00 PM	4:20 PM	D2. Interconnection Technologies 2	Veranda II	Prof Seungbae Park, Binghamton University
12/05/2024	3:00 PM	4:20 PM	D3. Materials and Processing 2	Veranda III	SS Kang, Heraeus Singapore
12/05/2024	3:00 PM	4:20 PM	D4. Mechanical Simulation & Characterization 2	RiverFront I	Prof Chiang Kuo Ning, National Tsing Hua University
12/06/2024	09:00 AM	10:20 AM	E1. Assembly and Manufacturing Technology 2	Veranda I	Mark Shaw, STMicroelectronics Italy
12/06/2024	09:00 AM	10:20 AM	E2. Wafer Processing and Characterization 2	Veranda II	Dr Toh Chin Hock, Apple
12/06/2024	09:00 AM	10:20 AM	E3. Materials and Processing 3	Veranda III	Prof Kim Sungdong, Seoul National University of Science
12/06/2024	09:00 AM	10:20 AM	E4. Mechanical Simulation & Characterization 3	RiverFront I	Sasi Kumar Tippabhotla, IME, Singapore
12/06/2024	09:00 AM	10:20 AM	E5. Quality, Reliability & Failure Analysis 1	RiverFront II	Prof Jeff Suhling, Auburn University
12/06/2024	09:00 AM	10:20 AM	E6. Silicon Interposer and Processing	RiverFront III	Dr Prayudi Lianto, Applied Materials
12/06/2024	10:35 AM	11:55 AM	F1. Automotive and Power Device Packages	Veranda I	Dr Tang Gongyue, IME Singapore
12/06/2024	10:35 AM	11:55 AM	F2. Quality, Reliability & Failure Analysis 2	Veranda II	Xue Ming, Infineon
12/06/2024	10:35 AM	11:55 AM	F3. Materials and Processing 4	Veranda III	Dr Alvin Lee, Brewer Science
12/06/2024	10:35 AM	11:55 AM	F4. Advanced Optoelectronics	RiverFront I	Vasarla Nagendra Sekhar, IME, Singapore
12/06/2024	10:35 AM	11:55 AM	F5. Electrical Simulations & Characterization 3	RiverFront II	Prof Bruce Kim, City University of New York
12/06/2024	10:35 AM	11:55 AM	F6. Thermal Management and Characterization 4	RiverFront III	Dr Refai-Ahmed Gamal, AMD
12/06/2024	12:55 PM	02:15 PM	G1. Bonding & Debonding Processes	Veranda I	Dr Viorel Dragoi, EV Group
12/06/2024	12:55 PM	02:15 PM	G2. Wafer Processing and Characterization 3	Veranda II	Clifford Sandstrom, Deca Technologies
12/06/2024	12:55 PM	02:15 PM	G3. Materials and Processing 5	Veranda III	DDr Alvin Lee, Brewer Science
12/06/2024	12:55 PM	02:15 PM	G4. Smart Manufacturing, Equipment & Tooling Co-Design	RiverFront I	Dangayach Sachin, Applied Materials
12/06/2024	12:55 PM	02:15 PM	G5. TSV & Wafer Level Packaging 3	RiverFront II	Vempati Srinivasa Rao, IME
12/06/2024	12:55 PM	02:15 PM	G6. Embedded and Fan-Out Packaging	RiverFront III	Dr Masahisa Fujino, IME Singapore
12/06/2024	2:30 PM	3:30 PM	H2. Quality, Reliability & Failure Analysis 3	Veranda II	David Gani, STMicroelectronics Singapore
12/06/2024	2:30 PM	3:30 PM	H3. Materials and Processing 6	Veranda III	Hemanth Kumar Cheemalamarri, IME Singapore
12/06/2024	2:30 PM	3:30 PM	H4. Mechanical Simulation & Characterization 4	RiverFront I	Rathin Mandal, IME Singapore
12/06/2024	2:30 PM	3:30 PM	H5. Advanced Chip and Package Designs	RiverFront II	Dr Kelly Brian, AMD
12/06/2024	2:30 PM	3:30 PM	H6. Flip Chip and Fan-out on Substrate	RiverFront III	Lee Chee Ping, Lam Research